Distributed Power System SA3000 Drive Configuration and Programming Version 1.2

M/N 57C653

Instruction Manual S-3042

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Reliance Electric

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D-C BUS CAPACITORS RETAIN HAZARDOUS VOLTAGES AFTER INPUT POWER HAS BEEN DISCONNECTED. AFTER DISCONNECTING INPUT POWER, WAIT TEN (10) MINUTES FOR THE D-C BUS CAPACITORS TO DISCHARGE. WHEN THE VOLTAGE IS DOWN TO ZERO (0) VOLTS, CHECK THE VOLTAGE WITH AN EXTERNAL VOLTMETER TO ENSURE THE D-C BUS CAPACITORS ARE DISCHARGED BEFORE TOUCHING ANY INTERNAL COMPONENTS. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN SEVERE BODILY INJURY OR LOSS OF LIFE.

WARNING

THE USER MUST PROVIDE AN EXTERNAL, HARDWIRED EMERGENCY STOP CIRCUIT OUTSIDE OF THE DRIVE CIRCUITRY. THIS CIRCUIT MUST DISABLE THE SYSTEM IN CASE OF IMPROPER OPERATION, UNCONTROLLED MACHINE OPERATION MAY RESULT IF THIS PROCEDURE IS NOT FOLLOWED, FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN BODILY INJURY.

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WARNING

REGISTERS AND BITS IN THE UDC MODULE THAT ARE DESCRIBED AS "READ ONLY" OR FOR "SYSTEM USE ONLY" MUST NOT BE WRITTEN TO BY THE USER. WRITING TO THESE REGISTERS AND BITS MAY RESULT IN IMPROPER SYSTEM OPERATION. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN BODILY INJURY.

CAUTION: Electronic motor overload protection must be provided for each motor in a Distributed Power drive application to protect the motor against excessive heat caused by high currents. This protection can be provided by either the THERMAL OVERLOAD software block or an external hardware device. Applications in which a single power module is controlling multiple motors cannot use the THERMAL OVERLOAD software block and must use an external hardware device or devices to provide this protection. Failure to observe this precaution could result in damage to, or destruction of, the equipment.

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1.0 INTRODUCTION

The products described in this manual are manufactured or distributed by Reliance Electric Industrial Company.

Distributed Power System (DPS) drives are controlled through coordination between:

- Tasks written by the programmer for the AutoMax[®] Processor
- Tasks written by the programmer for the Universal Drive Controller (UDC) module
- The control algorithm and a number of software routines executed by the Power Module Interface (PMI)

The data and commands required by the PMI operating system to carry out its functions are provided by the programmer through the AutoMax rack configuration and the UDC task. The programmer provides this information by:

- Entering the drive parameters
- Configuring the registers in the UDC module
- Defining the values of the pre-defined local tunables.
- Writing the UDC task

This manual describes the configuration and programming necessary to control SA3000 drives. Refer to the publications listed in section 1.1 for detailed descriptions of the hardware components of an SA3000 drive system.

The AutoMax Programming Executive V3.4 (M/N 57C345, 57C346, 57C395, and 57C397) or later is required to support the \$A3000 drive. Beginning with V3.5 Executive software, drive regulators are sold separately. The AutoMax Programming Executive instruction manual describes the Programming Executive software in detail.

This instruction manual assumes that you are familiar with the AutoMax Programming Executive software and makes references to it throughout. This manual does not describe specific applications of the standard hardware and software.

1.1 Related Publications

Refer to the following Reliance Electric instruction manuals as needed:

- S-3005 Distributed Power System Overview
- S-3007 Distributed Power System Universal Drive Controller Module
- S-3009 Distributed Power System Fiber-Optic Cabling
- S-3020 Distributed Power System Medium Power SA3000 A-C Power Modules
- S-3021 Distributed Power System SA3000 Diagnostics, Troubleshooting, and Start-Up Guidelines
- S-3023 Distributed Power System SA3000 Information Guide
- S-3029 Distributed Power System High Power SA3000 A-C Power Modules
- S-3019 Distributed Power System SA3000 Power Module Interface Rack.
- AutoMax Programming Executive Version 3.4 or later

2.0 CONFIGURING THE UDC MODULE, REGULATOR TYPE, AND PARAMETERS

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The Rack Configurator application in the AutoMax Programming Executive is used to configure the modules in a rack. Using the Rack Configurator, you create a graphical representation of the actual modules in the rack. Refer to of the AutoMax Programming Executive instruction manual for more information on configuring racks.

You can access the Rack Configurator by selecting the Configure Rack option from the Rack menu of the System Configurator. An empty AutoMax rack will be displayed initially.

2.1 Adding a UDC Module

The UDC module may be placed in any slot in an AutoMax rack that contains at least one AutoMax Processor module (M/N 57C430A, 57C431, or 57C435). Note that the UDC module cannot be used in a remote I/O rack. The rack does not require a Common Memory module (M/N 57C413 or 57C423) unless more than one AutoMax Processor is being used. A rack may contain up to ten UDC modules.

Some AutoMax modules, e.g., the Common Memory module and the Ethernet." Interface module, may have an effect on the slot allocation in the rack that limits where other modules may be inserted. Refer to the appropriate instruction manual for additional information. A UDC module may also be placed in a rack containing a set of the AutoMax drive controller modules (B/M 57401, 57405, 57406, and 57408).

Use the following procedure to add a UDC module to a rack:

- Step 1. Select an empty slot in the rack.
- Step 2. Select Add from the Configure menu. A dialog box listing the available modules will be displayed on the screen.
- Step 3. Select the UDC module.
- Step 4. Select a product type and a regulator (control) type for both drive A and drive B. See section 2.1.1 for regulator selection rules. The remainder of this chapter assumes you have selected SA3000 or SA3000 Parallel Inverters as the product type.
- Step 5. Select OK to add the UDC module to the rack and return to the Rack Configurator screen.

2.1.1 Rules for Configuring/Selecting Drives for the UDC Module

- 1. Both A and B drives do not have to be used. (You can configure only one.)
- Your A/B drive type combination is restricted only if you select an SD3000 (12-Pulse) drive, an SF3000 drive, or an SA3000 Parallel Inverters drive for either drive A or drive B. For these products, you are restricted to the drive type combinations shown in the table below. All other drive type combinations are allowed.

If you choose for Drive A	Then your choices for Drive B are	
SD3000 (12-Pulse)	SD3000 12-Pulse Auxiliary	
SF3000	No PMI Attached SD3000 (6-Pulse) SF3000	
SA3000 Parallel Inveners	SA3000 Parallel Inverters Auxiliary	

2.2 Entering the Drive Parameters

Drive parameters are application-specific data that describe your installation's Power Modules, foodback devices, and motors. This information is loaded to the UDC module, which in turn automatically downloads it to the PMI when the two are first connected over the fiber-optic link. This information is also stored off-line with the Programming Executive. Note that the drive parameters will be retained by the UDC module during a Stop All fault or command in the rack.

Once a UDC module has been added to the rack, use the **Zoom In** command to begin entering the drive parameters. Refer to the AutoMax Programming Executive instruction manual for more information on **Zooming** in and out.

Use the following procedure to enter the drive parameters. Section 2.6 describes how to load the drive parameter files when you are finished. Note that if you enter drive parameter data that is unexpected or out of range, a "warning" or "error" message will appear on the screen. A warning message indicates that the data you have just entered will be accepted by the Programming Executive, and you will be able to generate drive parameter files; however, you may experience degradation of drive performance. An error message indicates that the data you have just entered is unacceptable, and you will not be able to generate drive parameter files.

Step 1. **Zoom** into the UDC module. The Power Module Interface (PMI) screen will be displayed. You can also access this screen cirectly by double-clicking the UDC module.

This screen shows either one or two PMI diagrams depending upon the information you previously entered. One diagram will be shown for drive A and one for drive B, if used.

Each PMI diagram will show two rail ports (0 and 1) and the analog or digital rails that are connected to the PMI. Initially, no rails are connected.

Only one drive can be selected at a time when two drives are shown on the screen:

- the Drive A option will make drive A the selected drive.
- the Drive B option will make drive B the selected drive.

Entered commands will only affect the selected drive.

Step 2. If a rail is to be connected to the PMI's rail ports, click the appropriate rail port, either 0 or 1. Select Add under the Configure menu to add the rail to the rail ports.

You can choose from the following rall devices:

- M/N 45C001 Digital I/O Rail
- M/N 45C630 4-Decade Thumbwheel Switch Input Module
- M/N 45C631 4-Digit LED Output Module
- M/N 61C345 4-Channel Analog Current Input Rail
- M/N 61C346 4-Channel Analog Voltage Input Pall

- M/N 61C350 2-Channel Analog Voltage Input/Output Rail
- M/N 61C351 2-Channel Analog Current Input/Output Rail
- M/N 61C365 4-Channel Analog Current Output Rail.
- M/N 61C366 4-Channel Analog Vollage Output Rail

The Location field can be used to identify the physical location of the I/O.

Click OK and the device will be added to the screen. If you are adding a digital I/O rail, you will need to configure the I/O modules that the rail contains. Double-click the rail to display the expanded digital I/O rail screen. To add an I/O module, select the module's slot by moving the cursor to it and clicking it. Select the **Add** option from the Configure menu for a list of the available modules. Select the appropriate module and click OK. **Zoom** out to return to the PMI screen (Back Configurator).

Note that you cannot attach a Local I/O Head to the PMI's rail ports. You can, however, mix input and output modules in a Digital I/O Rail. You can also mix rail types, i.e., add both a Digital I/O Rail and an Analog Rail (rail mode only) to a PMI.

Select the Configure Variables option from the Configure menu in order to configure the variables for the attached rails. **Zoom** out to return to the PMI screen.

Step 3. Use the Configure Parameters option to access the Parameter Entry screens. Assuming you are configuring an SA3000 drive, there are four screen displays: Power Module Data, Motor Data, Feedback Data, and Meter Port Selection. See figure 2.1. Each of these screens is described in detail in the following sections (section 2.3 for Vector, sections 2.2.5 through 2.4 for Vector with Constant Power).

Note that the AutoMax slot number of the UDC module is shown at the top of the screens. The screens prompt for specific information depending upon the item that is being configured.

Step 4. When you have made entries for the drive parameters on all of the parameter entry screens, you should select the "Verify" option displayed at the bottom of the screen. If any of the values you entered are invatid or out of range, the parameter that is invalid will be highlighted so that you can change the value. When you have finished entering drive parameters, select "Save" to save the values to the database.

Conven	This area contains specific carameter data about the selected device.
Power Module Cata	
O Feedback Data	
J	

Figure 2.1 - SA3000 (Vector) Drive Parameter Entry Screen

2.3 Using the Vector Parameter Entry Screens (Product Type: SA3000)

The following sections describe the parameter entry screens for the SA3000 Vector regulator. These screens are accessed by selecting SA3000 as the product type and Vector as the regulator type when configuring the UDC module.

2.3.1 Power Module Data Screen (Vector)

The Power Module Data screen allows you to enter specific information about your power system configuration and the type of the Power Module being used. See figure 2.2.

● D.ive 7 O D.ive 7	OD Insta Willinge O AC Input Votage 800
New Fower Mcdule Data Mater Data Feedback Data Meter Part Selection	Power Madule Part Number: ScS412-4 (pr4-)(22KHz) 776 VDC m Camler Frequency (KHz): 2.0 Max. Amps 3: 2.0 KHz = 66 Amps
	Max, Amps at 20 KH-z = 66 Amps

Figure 2.2 - Power Module Data Parameter Entry Screen (Vector)

Power System Configuration Selections

D-C Input Voltage or A-C Input Voltage

Select the type of input line voltage (A-C input or D-C input) and then enter the input voltage value.

Select D-C Input Voltage if this is the D-C bus voltage. Select A-C Input Voltage if this is the A-C RMS voltage that is being converted to D-C bus voltage. The default selection is D C Input Voltage.

MCR Connected To Output Contactor

If you have a motor control relay (MCR) on the output of the inverter (output contactor), select this option. If there is only a manual disconnect switch and no contactor under automatic control, do not select the output contactor option. The default selection is to not have an output contactor.

Power Module

Part Number

Select a part number from the list of supported Power Modules. The current ratings in the list are the rated RMS currents at a 2 kHz switching frequency with no overload at 40° ambient. There is no default selection. You must choose a part number from the list.

The Power Module must be able to operate at the voltage level selected for the input Voltage parameter above. An error message will be issued if the line voltage value entered is not within the range shown in Appendix F. Refer to the appropriate SA3000 Power Module instruction manual for more information.

Carrier Frequency

The carrier frequency selected will determine the switching frequency of the Power Module. You can select from a list of the preset carrier frequencies: 2 kHz (datault), 4 kHz, 6 kHz, 8 kHz, or 10 kHz, or you can enter a value between 2 kHz and 16 kHz in increments of 100 Hz. The hardware in some cases will have slightly coarser resolution at the higher frequencies. Refer to Appendix F for the carrier frequency limit for the Power Module you have selected.

All Power Modules are rated at the 2 kHz switching irequency but they can be operated above this limit by de-rating the unit's output.

2.3.2 Motor Data Screen (Vector)

The Motor Data parameter screen allows you to enter specific information about the motor you are using. (If you are using a high stip motor, refer to Appendix B for additional information.) See figure 2.3.

Dive A O Crive B	Hated Power	HP OKW	15.0
- View	Ratec Motor Voltage	(Vols RMS):	200
Power Module Data Motor Data	Rated Molor Current	(Amps AMS):	42.0
Feedback Data Meter Port Selection	Iorque Overload Ratio	(%):	140
L <u></u>	Freq. or Rated Voltage	()Hz;	60
	Pated Full Load Speed	(NPN):	1172
	Motor Poles (calculated value	ie = 0):	6 💓

Figure 2.3 - Motor Data Parameter Entry Screen (Vector)

Rated Power (Range: 1 HP to 1600 HP or 1 KW to 1200 KW)

Enter the power rating of the motor and select HP (default) or KW. There is no default value. NOTE: HP to KW conversion is 1 HP = 0.746 KW.

Rated Motor Voltage (Volts RMS) (Range: 100V to 575V)

Enter the rated RMS motor voltage. There is no default value. A warning message will be displayed if the value entered is less than 50% or greater than 100% of the A-C input Voltage parameter. (Note that if the input voltage is entered as D-C, it is converted to A-C by the system for this test.)

Rated Motor Current (Amps RMS) (Range: 1.0A to 3000.0A)

Enter the rated RMS motor current exactly as it appears on the motor nameplate. The resolution is 0.1 amp. There is no default value. This value can range from 25% to 100% of the Power Module's rating at the selected carrier frequency.

Torque Overload Ratio (%) (Range: 25 to 400)

The Torque Overload Ratio determines the maximum RMS current that can be supplied to the motor by the Power Module. The ratio affects only the Iq (lorque) component of RMS current to the motor. Enter the torque overload ratio in percent of rated motor torque, which can be calculated from the rated speed and HP. For example, 150% of rated motor torque is enlered as 150. The default value is 100. The resolution is 1%. See Appendix E for how to calculate the effect of the ratio on maximum RMS current.

A warning will be generated if the following condition is not met:

Rated Motor Current * (Torque Overload Ratio(100) <= Power Module Rated Amps at Selected Carrier Prequency

If a warning appears, it is likely that the maximum RMS current that can be supplied to the motor at the torque overload ratio level selected is too high for the Power Module selected. Refer to Appendix E for more information on determining the maximum RMS current that will result from the ratio entered.

Frequency at Rated Voltage (Hz) (Range: 1 to 400)

This value is used to determine the frequency at which the motor enters the constant power range. Enter the value in hertz. The resolution is 1 Hz. There is no default value.

Rated Full Load Speed (RPM) (Range: 10 to 10,000)

This value is used to determine the rated slip of the motor at the rated motor frequency. This value is found on the motor's nameplate. Enter the value in RPM; the resolution is 1 RPM. There is no default value.

Motor Poles (2, 4, 6, 8, 10, 12, 14, or 16)

This value is used to determine the relationship between drive output frequency and motor shaft speed. Because this number is not readily available, the number of motor poles will be calculated automatically based on the other parameters you have entered and will be displayed on the screen. You must then select this calculated value from a list of the preset values. There is no default value.

The following formula will be used to calculate the number of motor poles:

120 * Frequency at Rated Voltage / Rated Full Load Speed

The resulting number will be rounded down to the nearest whole even number. Note that this formula may not result in the correct number of motor poles if you are using a high slip motor, such as a NEMA design D motor. Refer to the following table for the maximum slip per number of motor poles that will result in a correct calculation.

Number of Poles	Maximum Slip
2	49%
4	33%
6	24%
8	19%
10	16%
12	14%

For example, on an 8-pole motor, if slip is greater than 19%, the calculated value will be incorrect. You must then enter the correct value.

2.3.3 Feedback Data Screen (Vector)

The Feedback Data parameter screen allows you to enter specific information about the resolver connected to the Resolver and Drive I/O module in the PMI rack. See figure 2.4.

	Over Speed Feedback Type
Power Module Data Votor Data () Feetback Data () Feetback Data () Meter Port Selection	Hescher Data Type: Officina ® x1 O x2 O x5 Resolution: @ 12 Bits O 14 Bits
	Control Selections Output Hetation: OVW OVW Datable UDC Flux Reference

Figure 2.4 - Feedback Data Parameter Entry Screen (Vector) with Resolver Selected

Over Speed Limit (RPM) (Range: 10 to 10,000)

This value is used to determine the maximum safe output frequency of the drive. There is no default value. Over Speed Limit should generally be equal to or less than the motor maximum safe speed or the driven equipment maximum safe speed, whichever is lower. If a value less than 1% of the motor's Rated Full Load Speed is entered, an error message will be generated.

Speed Feedback Type

You must select Resolver. The No Speed Feedback option is not allowed for vector regulators.

Resolver Data

Resolver Type

Select the resolver type from the three choices: x1, x2, or x5. The "None" option is not allowed for vector regulators. The resolver selected must be able to operate at the Over Speed Limit of the motor.

Resolution

This value is used to configure the Resolver & Drive I/O module (B/M O-60031) for either 12 bit or 14-bit conversion of the resolver data. The 12-bit mode is designed to be used with the following Reliance resolvers:

Resolver Base Part No.	×1	x2	x5
	Suffix		
613469	-1R		1 100 100 100 100 100 100 100 100 100 1
613469	-15		
613469	-2R	er enwenen enve	
613469	-25		
800123	-R	-S	-T
800123	_1R	-1\$	-1T
800123	-2R	-2S	-2T

Currently there are no Reliance resolvers that support the 14-bit mode.

For the most accurate velocity control, always select the resolver (x1, x2, or x5) whose maximum speed is closest to, and greater than, the maximum speed of your application. Refer to the SA3000 PMI Rack instruction manual for more information regarding the Resolver & Drive I/O module and the supported resolvers.

Control Selections

Output Rotation

This parameter allows you to reverse the direction of rotation of the output without re-wiring the motor leads. Select UVW (default) or UWV. Note that the resolver cosine connections must also be interchanged. Refer to the SA3000 Diagnostics, Troubleshooting, and Start-Up Guidelines instruction manual for more information on motor orientation.

Enable UDC Flux Reference

Check this box if you want to provide a flux reference to the PMI via the UDC in place of that calculated by the PMI.

You may want to select this parameter for the following reasons:

- To control the flux reference for motors that do not produce constant flux in the constant torque range (i.e., below base speed).
- To control motor speed in the constant power region up to a range of 2:1; that is, up to two times base speed.

The value in register 104/1104 (FLX_REF%) is then used as the ratio for scaling the value for magnetizing current (STATOR_IZ_E1%). For example, if register 104=4095, then the full value of STATOR_IZ_E1% will be used for magnetizing current.

If this box is not checked, magnetizing current is equal to the value in tunable STATOR_IZ_E1%. This is the default selection.

2.3.4 PMI Meter Port Selection Screen (Vector)

The Moter Port Selection parameter screen allows you to enter specific information about what variables are to be output on the four PMI D/A channels (the four "moter" ports on the PMI Processor module). See figure 2.5.



Figure 2.5 - Meter Port Selection Entry Screen (Vector)

Figure 2.6 shows the values that can be displayed on the PMI meter ports. You must enter a Minimum Value and a Maximum Value for each selection except when you select Port Not Used. The Minimum Value is the value at which to output -10V. The Maximum Value is the value at which to output +10V. The system software then places the units per volt on the screen based on the Minimum/Maximum Values. The Minimum Value must not be less than -32768. The Maximum Value must not be greater than 32767. The Minimum Value must be less than the Maximum Value. Note that the PMI meter ports have 8-bit resolution and are updated on the average every 1.0 millisecond. Refer to the Power Module Interface Rack instruction manual for more information about the PMI meter ports. Refer to section 3.6.2.1 for information about resolution of data.

- Port Not Used
- Torque Reference (+/- 4095 = Full Torque)
- Torque Feedback (+/- 4095 = Full Torque)
- D-C Bus Voltage (Volts)
- D-C Bus Current (Amps x 10)
- Ground Fault Current (Amps x 10)
- Motor Voltage Feedback (Volts)
- Motor Current Feedback (Amps x 10)
- Id Current Reference (-2047 = -IOC, 0 = 0V, 2047 = +IOC)
- Id Current Feedback (-2047 = -IOC, 0 = 0V, 2047 = +IOC)
- Vd Reference (-2047 = max. neg. output of current loop, 0 = 0V, 2047 = max. pos. output of current loop)
- Iq Current Reference (-2047 = -IOC, 0 = 0V, 2047 = +IOC)

- Iq Current Feedback (-2047 = -10C, 0 - 0V, 2047 - +10C)
- Vq Reference (-2047 = max. neg. output of current loop, 0 = 0V, 2047 = max. pos. output of current loop)
- Slip Frequency (Hz x 100)
- Output Frequency (Hz x 10)
- User Analog Input (Counts)
- Speed Feedback (RPM)
- Application Data (Units)
- Rail Port 0 Channel 0 (Counts)
- Rail Port 0 Channel 1 (Counts)
- Rail Port 0 Channel 2 (Counts)
- Rail Port 0 Channel 3 (Counts)
- Rail Port 1 Channel 0 (Counts)
- Rail Port 1 Channel 1 (Counts)
- Rall Port 1 Channel 2 (Counts)
- Rail Port 1 Channel 3 (Counts)

NOTE: Power Module IOC = Power Module peak rated current x 1.25 (for Power Module part numbers 805xx only). Power Module peak rated current = Power Module rated RMS current x √2. Output frequency is bipolar and is negative for reverse rotation.

<u>*</u>0

Figure 2.6 - PMI Meter Port Parameters (Vector)

PMI meter ports can also be set up on-line using the "Setup UDC" selection from the Monitor menu as described in the AutoMax Programming Executive instruction manual. If the meter ports are set up during parameter entry, the information is loaded onto the UDC module in the AutoMax rack along with all other parameter data. The meter port setup can then be changed on-line under "Setup UDC", but this method would not actually write over the PMI meter port setup that was loaded to the rack. Instead, the new setup would be valid only until there was a Stop All or a power cyclo, in which case the original setup would be used to determine what data to send out of the meter ports.

2.4 Using the Vector with Constant Power Parameter Entry Screens (Product Type: SA3000, SA3000 Parallel Inverters)

The following sections describe the parameter entry screens for the Vector with Constant Power regulator. These screens are accessed by selecting either SA3000 or SA3000 Parallel Inverters as the product type and Vector with Constant Power as the regulator type when configuring the UDC module.

If you have selected SA3000 Parallel Inverters, you can enter the drive parameters for drive A only. The system will automatically process and copy the data for drive B from the drive A data. The PMI D/A meter ports, however, can still be configured for drive B.

Note that if you have selected SA3000 Parallel Inverters, the title bar at the top of each screen will read SA3000 (Vector - Parallel Inverters).

2.4.1 Power Module Data Screen (Vector with Constant Power)

The Power Module Data screen allows you to enter specific information about your power system configuration and the type of Power Module being used. See figure 2.7.

UDC Drive B Drive B Vlaw Power Wedulk Dazz Mater Data Foothack Dazz Mater Port Sciection	Power System Configuration DC riput Voltage AC Input Voltage BC MCR Connected To Output Consider Power Module Part Number: (05112-25 (1/ Amps 6)25116) 775 v00m (1/) Carrier Frequency (KHz): 2.0
<u>1986</u>	n <u>assessa</u>

Figure 2.7 - Power Module Data Parameter Entry Screen (Vector with Constant Power)

Power System Configuration Selections

D-C input Voltage or A-C input Voltage

Select the type of input line voltage (A-C input or D-C input) and then enter the input voltage value.

Select D-C Input Voltage if this is the D-C bus voltage. Select A-C Input Voltage if this is the A-C RMS voltage that is being converted to D-C bus voltage. The default selection is D-C Input Voltage.

MCR Connected to Output Contactor

If you have a motor control relay (MCR) on the output of the inverter (output contactor), select this option. If there is only a manual disconnect switch and no contactor under automatic control, do not select the output contactor option. The default selection is to not have an output contactor.

Power Module

Part Number

Select a part number from the list of supported Power Modules. The current ratings in the list are the rated RMS currents at a 2 kHz switching frequency with no overload at 40° ambient. There is no default selection. You must choose a part number from the list.

The Power Module must be able to operate at the voltage level selected for the input Voltage parameter above. An error message will be issued if the line voltage value entered is not within the range shown in Appendix F. Refer to the appropriate SA3000 Power Module instruction manual for more information.

Carrier Frequency

The carrier frequency selected will determine the Power Module's switching frequency. You can select from a list of the preset carrier frequencies: 2 kHz (default), 4 kHz, 6 kHz, 8 kHz, or 10 kHz; or you can enter a value between 2 kHz and 16 kHz in increments of 100 Hz. The hardware in some cases will have slightly coarser resolution at the higher frequencies. Refer to Appendix F for the carrier frequency limit for the Power Module you have selected.

All Power Modules are rated at the 2 kHz switching frequency, but they can be operated above this limit by de-rating the unit's output.

2.4.2 Motor Data Screen (Vector With Constant Power)

The Motor Data parameter screen allows you to enter specific information about the motor you are using. (If you are using a high slip motor, refer to Appendix B for additional information.)

	Magnadzation Compensation Form	istant- ier
View	Rated Power Image HP Image KW: Imag	15.0 180 19.0 130 60.0 1785 4

Figure 2.8 - Motor Data Parameter Entry Screen used for Constant Magnetization or Manual Compensation

Constant Magnetization, Manual Compensation, or Constant Power

These selections define the method the system will use to determine the value used for magnetizing current in the control algorithm.

The default selection for SA3000 drives is Constant Magnetizing Current where the value stored in local tunable STATOR_IZ_E1% is used for the magnetizing current value. The PMI Processor calculates this value in response to the PMI_TUN@ command. Select Manual Compensation to allow operation in the constant power region up to 2:1. In this case, the value in register 104/1104 (FLX_REF%) is used to scale STATOR_IZ_E1% where 4095 equals full magnetizing current.

Select Constant Power to allow operation in the constant power region up to 4:1. In this case, the PMI Processor calculates magnetizing current using motor voltage feedback (flux loop). This is the default selection for SA3000 Parallel Inverters. See section 2.4.2.1 for the Constant Power Motor Data Screen description for Parallel Inverters.

For the first two selections, you will need to supply the following information as shown in figure 2.8:

Rated Power (Range 1 HP to 1600 HP or 1KW to 1200 KW)

Enter the power rating of the motor and select HP (default) or KW. There is no default value.

NOTE: HP to KW conversion is 1 HP = 0.746 KW.

Rated Motor Vollage (Volts RMS) (Range: 100V to 575V)

Enter the rated RMS motor voltage. There is no default value. A warning message will be displayed if the value entered is less than 60% or greater than 100% of the A-C Input Voltage parameter. (Note that if the input voltage was entered as D-C, it is converted to A-C by the system for this test.)

Rated Motor Current (Amps RMS) (Range: 1.0A to 3000.0A)

Enter the rated RMS motor current exactly as it appears on the motor nameplate. The resolution is 0.1 amp. There is no default value. This value can range from 25% to 100% of the Power Module's rating at the selected carrier frequency.

Torque Overload Ratio (%) (Range: 25 to 400)

The Torque Overload Ratio determines the maximum RMS current that can be supplied to the motor by the Power Module. The ratio affects only the Iq (torque) component of RMS current to the motor. Enter the torque overload ratio in percent of rated motor torque, which can be calculated from the rated speed and HP. For example, 150% of rated motor torque is entered as 150. The default value is 100. The resolution is 1%. See Appendix E for how to calculate the effect of the ratio on maximum RMS current.

A warning will be generated if the following condition is not met:

Rated Motor Current * (Torque Overload Ratio/100) <= Power Module Rated Amos at Selected Carrier Frequency

If a warning appears, it is likely that the maximum RMS current that can be supplied to the motor at the torque overload ratio level selected is too high for the Power Module selected. Refer to Appendix E for more information on determining the maximum RMS current that will result from the ratio entered.

Frequency at Rated Voltage (Hz) (Range: 1 to 400)

This value is used to determine the frequency at which the motor enters the constant power range. Enter the value in hertz. The resolution is 0.1 Hz. There is no default value.

Rated Full Load Speed (RPM) (Range: 10 to 10,000)

This value is used to determine the rated slip of the motor at the rated motor frequency. This value is found on the motor's nameplate. Enter the value in RPM; the resolution is 1 RPM. There is no default value.

Motor Poles (2, 4, 6, 8, 10, 12, 14, or 16)

This value is used to determine the relationship between drive output frequency and motor shaft speed. Because this number is not readily available, the number of motor poles will be calculated automatically based on the other parameters you have entered and will be displayed on the screen. You must then select this calculated value from a list of the preset values. There is no default value.

The following formula will be used to calculate the number of motor poles:

120 * Frequency at Rated Voltage / Rated Full Load Speed

The resulting number will be rounded down to the nearest whole even number. Note that this formula may not result in the correct number of motor poles if you are using a high slip motor, such as a NEMA design D motor. Refer to the following table for the maximum slip per number of motor poles that will result in a correct calculation.

Number of Poles	Maximum Slip	3
2	49%	2
4	39%	- 8
6	24%	3
8	19%	1
10	16%	
12	14%	

For example, on an 8-pole motor, if slip is greater than 19%, the calculated value will be incorrect. You must then enter the correct value.

2.4.2.1 Constant Power Motor Data Screen (Vector With Constant Power)

When Constant Power is selected, a new screen is displayed, and the following information must be entered. See figure 2.9. Note that for SA3000 Parallel Inverters, this is the default Motor Data parameter entry screen.

● Drive Δ O Drive B ● Drive Δ O Drive B New Based Powsr ● Powar Module Data Maxemum Mater Vettage ● Powar Module Data Noter Data ● Feedback Data Based (RPM) ● Mater Port Selection Select 314 ● String Points 0 Vetto 35 ● String Points 0 Vetto 35 ● Selection Select 314 ● String Points 0 Vetto 35 ● String Points 0 Vetto 35 ● String Points 0 Vetto 35 ● Selection String Points ● String Points 0 Vetto 35 ● String Points 0 Vetto 35 ● Selection String Points ● String Point Selection 0 Vetto 35
\$2 700 C2 286 C2 160 \$2 1100 C3: 236 C3: 340 \$4 1200 : C4 230 C4 120 Free. at Rated Voltage (Hz): 25 25 Motor Poles (calculated value = 4): 4 190

Figure 2.9 - Motor Data Parameter Entry Screen used for Constant Power

Rated Power (Range: 1 HP to 1600 HP or 1KW to 1200 KW)

Enter the power rating of the motor and select HP (default) or KW. There is no default value. NOTE: HP to KW conversion is 1 HP = 0.746 KW.

Rated Motor Voltage (Volts RMS) (Range: 100V to 575V)

Enter the rated RMS motor voltage. There is no detault value. A warning message will be displayed if the value entered is less than 50% or greater than 100% of VAC.

Maximum Motor Voltage (Volta RMS) (Range: 100V to \$75V)

Enter the maximum RMS motor voltage. There is no default value. In motor designs where motor voltage reaches its maximum value at rated speed, this value will be equal to value entered in the Rated Motor Voltage parameter.

In motor designs where motor voltage continues to rise after reaching rated speed, this value will be greater than the value entered in the Rated Motor Voltage parameter. This information is found on the motor design data sheet.

Total Current Rating Points: (Range: 1 to 5)

This value is used to determine the number of rows that will be displayed in the following three parameter columns (Speed, Current, and Overload). When operating above base (rated) speed, the current and overload ratio may change. This selection allows the display of base values and up to four additional sets of data. Each data set represents consistent motor design data for one operating point of the motor. The number of additional points required is dependent upon the motor design. In most cases you will not need to use all five rows. See Appendix G for an example.

Speed (RPM) (Range: 10 to 10,000)

Enter all speed values in RPM; the resolution is 1 RPM. There are no default values.

Base: Enter the base (rated) speed of the motor. The base speed value represents the speed where the motor enters the constant power region. This value is used to determine the rated slip of the motor at the rated motor frequency. This value is found on the motor's nameplate.

S1: Enter the speed at which maximum voltage is reached. If the rated voltage is not equal to the maximum voltage of the motor, the PMI Processor will automatically calculate the value of S1 when you select "Verify." If rated voltage and maximum voltage are the same, you must enter this value manually. This information is located on the motor design data sheet.

S2-S4: Enter additional speed values as required by the motor design. The additional speed values represent taper points of the constant power region. Note that the additional speed values cannot be greater than 4 times the speed at maximum motor voltage.

Current (Amps)

Enter all current values in amps; the resolution is 0.1 amp. This value can range from 25% to 100% of the Power Module's rating at the selected carrier frequency.

Base: Enter the base (rated) RMS motor current exactly as it appears on the motor namepla:e. There is no default value.

C1-C4; Enter additional current values at each speed (e.g., C1 corresponds to the motor current level at speed S1.) This information is located on the motor design data sheet.

Torque Overload Ratio (%) (Range: 25 to 400)

The Torque Overload Ratio determines the maximum RMS current that can be supplied to the motor by the Power Module. The ratio affects only the Iq (torque) component of RMS current to the motor. Enter the torque overload ratio in percent of rated motor torque, which can be calculated from the rated speed and HP. For example, 150% of rated motor torque is entered as 150. The default value is 100. The resolution is 1%. See Appendix E for how to calculate the effect of the ratio on maximum RMS current.

A warning will be generated if the following condition is not met:

Reted Motor Current* (Torque Overkao Ratio/100) < = Power Modele Rated Amps at Carrier Frequency

Note that the Power Module Rated Amps at Carrier Frequency value is based on either the carrier frequency selected during parameter entry or the carrier frequency calculated by the system, whichever is greater. The carrier frequency is calculated by the system using the following equation:

Calculated carter frequency = 20 * (Freq. at Rated Voltage * Max. Speed/Base Speed)

If a warning appears, it is likely that the maximum RMS current that can be supplied to the motor at the torque overload ratio level selected is too high for the Power Module selected. Refer to Appendix E for more information on determining the maximum RMS current that will result from the ratio entered.

Base: Enter the base (rated) torque overload ratio.

O1-O4: Enter additional overload ratios at each speed. This information is located on the motor design data sheet.

Frequency at Rated Voltage (Hz) (Range: 1 to 400)

This value is used to determine the frequency at which the motor enters the constant horsepower range. The resolution is 0.1 Hz. There is no default value.

Motor Poles (2, 4, 6, 8, 10, 12, 14, or 16)

This value is used to determine the relationship between drive output frequency and motor shaft speed. Because this number is not readily available, the number of motor poles will be calculated automatically based on the other parameters you have entered and will be displayed on the screen. You must then select this calculated value from a list of the preset values. There is no default value.

The following formula will be used to calculate the number of motor poles:

120 * Frequency at Rated Voltage / Rated Full Load Speed

The resulting number will be rounded down to the nearest whole even number. Note that this formula may not result in the correct number of motor poles if you are using a high slip motor, such as a NEMA design D motor. Refer to the following table for the maximum slip per number of motor poles that will result in a correct calculation.

Number of Poles	Maximum Slip
2	49%
4	33%
6	24%
8	19%
10	16%
12	14%

For example, on an 8-pole motor, if slip is greater than 19%, the calculated value will be incorract. You must then enter the correct value.

2.4.3 Feedback Data Screen (Vector With Constant Power)

The Feedback Data parameter screen allows you to enter specific information about the resolver connected to the Resolver and Drive I/O module in the PMI rack. See figure 2.10.

	Over Speed Limit (RPM): 1175 Speed Feedback Type Oric Speed readouts () Resolver
Motor Base Motor Port Selection Motor Port Selection	Register Data Type: Norta Type: Norta Fosalution: 12.3Hs 14 Bits
	Comital Selections Colput Potesson:

Figure 2.10 - Feedback Data Parameter Entry Screen (Vector with Constant Power) with Resolver Selected

Over Speed Limit (RPM) (Range: 10 to 10,000)

This value is used to determine the maximum safe output frequency of the drive. There is no default value. Over Speed Limit should generally be equal to or less than the motor maximum safe speed or the driven equipment maximum safe speed, whichever is lower. If a value less than 1% of the motor's Rated Full Load Speed is entered, an error message will be generated.

Speed Feedback Type

You must select Resolver. The No Speed Feedback option is not allowed for vector regulators.

Bosolver Data

Resolver Type

Select the resolver type from the three choices: x1, x2, or x5. The "None" option is not allowed for vector regulators. The resolver selected must be able to operate at the Over Speed Limit of the motor.

Resolution

This value is used to configure the Resolver & Drive I/O module (B/M O-60031) for either 12-bit or 14-bit conversion of the resolver data. The 12-bit mode is designed to be used with the following Reliance resolvers:

Resolver	x1	x2	Х5		
Base Part No.	Suffix				
613469	-18		l 10		
613469	-15				
613469	-2R	W/S			
613469	-25				
800123	-R	-S	T		
600123	-1R	-1\$	-1T		
800123	-2R	-28	-5L		

Currently there are no Reliance resolvers that support the 14-bit mode.

For the most accurate velocity control, always select the resolver (x1, x2, or x5) whose maximum speed is closest to, and greater than, the maximum speed of your application. Refer to the SA3000 PMI Rack instruction manual for more information regarding the Resolver & Drive I/O module and the supported resolvers.

Control Selections

Output Rotation

This parameter allows you to reverse the direction of rotation of the output without re-wiring the motor feads. Select UVW (default) or UWV. Note that the resolver cosine connections must also be interchanged. Refer to the \$A3000 Diagnostics, Troubleshooting, and Start-Up Guidelines instruction manual for more information on motor orientation.

2.4.4 PMI Meter Port Selection Screen (Vector With Constant Power)

The Mater Port Selection parameter screen allows you to enter specific information about what variables are to be output on the four PMI D/A channels (the four "meter" ports on the PMI Processor module). See figure 2.11.

	Webus @ -10% 32500 value @ -10% 32500 25.80 Units/Veit 0.0 Units at 0 V
Power Module Ceta Vicor Dana Norr Dana Feedback Deta Vister Port Selection	Meter Port #2: Torque Feerlback (County) Value @ -10% -32500 Value @ -10% 32500 S5.80 Units/Volt 0.3 Units at 0 V Meter Port #3: DC 54.8 Voltage (Volta) 100 Value @ -10% 0 Volta 204.75 Units at 0 V Value @ -10% 0 Volta 2047.5 Units at 0 V Meter Port #4: Port Not Used 100 100

Figure 2.11 - Meter Port Selection Entry Screen (Vector with Constant Power)

Figure 2.12 shows the values that can be displayed on the PMI meter ports. You must enter a Minimum Value and a Maximum Value for each selection except when you select Port Not Used. The Minimum Value is the value at which to output -10V. The Maximum Value is the value at which to output +10V. The system software then places the units per volt on the screen based on the Minimum/Maximum Values. The Minimum Value must not be fess than -32768. The Maximum Value must not be greater than 32767. The Minimum Value must be less than the Maximum Value. Note that the PMI meter ports have 8-bit resolution and are updated on the average every 1.0 millisecond. Refer to the Power Module Interface Rack instruction manual for more information about the PMI meter ports. Refer to section 3.6.2.1 for information about resolution of data.

- Port Not Used
- Torque Reference (+/- 4095 = Full Torque)
- Torque Feedback
 (+/- 4095 = Full Torque)
- Flux Reference (1000 = 1 Hz)
- Flux Feedback (1000 = 1 Hz)
- D-C Bus Voltage (Volts)
- D-C Bus Current (Amps x 10)
- Ground Fault Current (Amps x 10)
- Motor Voltage Feedback (Volts)
- Motor Current Feedback (Amps x 10)
- Id Current Reference (-2047 = -IOC, 0 = 0V, 2047 = +IOC)
- Id Current Feedback (--2047 = -10C, 0 - 0V, 2047 = +10C)
- Vd Reference (-2047 = max. rag. output of current loop, 0 = 0V, 2047 = max. pos. output of current loop)

- Iq Current Reference (-2047 = -10C, 0 = 0V, 2047 - +10C)
- Iq Current Feedback (-2047 = -IDC, 0 = 0V, 2047 = +IOC)
- Vq Reference (-2047 + max. neg. output of current loop, 0 = 0V, 2047 = max. pos. output of current loop)
- Slip Frequency (Hz x 100)
- Output Frequency (Hz x 10)
- User Analog Input (Counts)
- Speed Feedback (RPM)
- Application Data (Units)
- Rail Port 0 Channel 0 (Counts)
- Rail Port 0 Channel 1 (Counts)
- Rail Port 0 Channel 2 (Counts)
- Rail Port 0 Channel 3 (Counts)
- Rail Port 1 Channel 0 (Counts)
- Rail Port 1 Channel 1 (Counts)
- Rail Port t Channel 2 (Counts)
- Rail Port 1 Channel 3 (Counts)
- Vector Angle (Counts)
- Vector Error (Counts)

NOTE: Power Module IOC = Power Module peak rated current x 1.25 (for Power Module part numbers 805xx only). Power Module peak rated current = Power Module rated RMS current x $\sqrt{2}$. Output frequency is bipolar and is negative for reverse rotation.

Figure 2.12 - PMI Meter Port Parameters (Vector with Constant Power)

PMI meter ports can also be set up on-line using the "Secup UDC" selection from the Monitor monu as described in the AutoMax Programming Executive instruction manual. If the meter ports are set up during parameter entry, the information is loaded onto the UDC module in the AutoMax rack along with all other parameter data. The meter port setup can then be changed on-line under "Setup UDC", but this method would not actually write over the PMI meter port setup that was loaded to the rack. Instead, the new setup would be valid only until there was a Stop All or a power cycle, in which case the original setup would be used to determine what data to send out of the meter ports.

2.5 Generating the Drive Parameter Files and Printing Drive Parameters

When you have completed all of the drive parameter screens, you can salect "Close" to leave the Parameter Entry screens and return to the master rack diagram with the UDC module selected. Zoom out or select the Exit command from the Configure menu to return to the System Configurator.

You can generate the drive parameter files by using the steps that follow.

- From the System Configurator, access the Task Manager by selecting the Manage Tasks command from the Pack menu.
- Step 2. Select the Generate Configuration command from the Commands menu.
- Step 3. Check the Generate Drive Parameter Files option in the Generate Files dialog box, and then select OK.

A file containing the newly-entered drive parameters will be created. The file will be named PARAMxx.POB, where xx is the slot number of the UDC module. Note that the drive parameter files must be loaded to the rack before (or at the same time) the UDC application tasks are loaded to the rack. Refer to the AutoMax Programming Executive instruction manual for more detailed information.

You can print the drive parameters for a UDC module you specify by using the Print command from the Reck menu in the System Configurator. Refer to the AutoMax Programming Executive instruction manual for step-by-step instructions

3.0 CONFIGURING THE UDC MODULE'S REGISTERS

DANGER

ONLY QUALIFIED ELECTRICAL PERSONNEL FAMILIAR WITH THE CONSTRUCTION AND OPERATION OF THIS EQUIPMENT AND THE HAZARDS INVOLVED SHOULD INSTALL, ADJUST, OPERATE, OR SERVICE THIS EQUIPMENT. READ AND UNDERSTAND THIS MANUAL AND OTHER APPLICABLE MANUALS IN THEIR ENTIRETY BEFORE PROCEEDING. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN SEVERE BODILY INJURY OR LOSS OF LIFE.

WARNING

ONLY QUALIFIED RELIANCE PERSONNEL OR OTHER TRAINED PERSONNEL WHO UNDERSTAND THE POTENTIAL HAZARDS INVOLVED MAY MAKE MODIFICATIONS TO THE VARIABLE CONFIGURATION. ANY MODIFICATIONS MAY RESULT IN UNCONTROLLED MACHINE OPERATION. FAILURE TO OBSERVE THESE PRECAUTIONS COULD RESULT IN DAMAGE TO EQUIPMENT AND BODILY INJURY.

WARNING

REGISTERS AND BITS IN THE UDC MODULE THAT ARE DESCRIBED AS "READ ONLY" OR FOR "SYSTEM USE ONLY" MUST NOT BE WRITTEN TO BY THE USER. WRITING TO THESE REGISTERS AND BITS MAY RESULT IN IMPROPER SYSTEM OPERATION. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN BODILY INJURY.

The Variable Configurator application in the AutoMax Programming Executive is used to assign common variable names to the dual port memory registers on the UDC module. You can access these variable names by declaring them using the BASIC statement COMMON. The dual port memory has 2048 16-bit registers that are available to the AutoMax Processor and to the tasks that run on the UDC module. The drive A and drive B registers that are assigned variable names will be latched into internal memory at the beginning of every scan of the UDC task to provide for a consistent context for evaluation. The UDC tasks (A and B) may be started and stopped independently of each other. At the end of the scan, the variables that have changed will be written back to the dual port memory. Note that the dual port memory on the UDC module is treated like I/O data in terms of how the data is affected by Stop All commands and power cycling.

You can access the Variable Configurator by selecting Configure Variables from the Configure menu in the Rack Configurator. Refer to the AutoMax Programming Executive instruction manual for the procedures used to configure variables.

The sections that follow describe the registers you can configure in each view:

- The Rail I/O Port 0 and Port 1 views are used to configure the registers assigned to the hardware that is attached to the PMI Rail ports. (These registers can also be accessed by double-clicking the PMI view.)
- The Command Registers view is used to configure pre-defined drive control registers that are written to either by an AutoMax application task or by a UDC application task and then sent to the PMI.
- The Feedback Registers view is used to configure the feedback registers that display the current status of the drive. These registers are written to by the PMI.
- The Application Registers Updated Every Scan view is used to configure the application registers that are used for the passing of application-specific control and status data between an AutoMax Processor and the UDC module on every scan. This register range is shared by drive A and drive B.

- The Application Registers Updated Every Nth Scan view is used to configure the application
 registers that are used for the passing of application-specific control and status data between an
 AutoMax Processor and the UDC module on every Nth scan, where "N" is defined in register
 2001. This register range is shared by drive A and drive B.
- The UDC Module Test I/O Register view is used to configure the register that displays the status
 of the UDC module's test switches and LED indicators. This view is also used to configure the
 UDC module's D/A meter ports.
- The Interrupt Status and Control Registers view is used to configure the registers that control a
 user-defined interrupt to an AutoMax task and enable the CCLK signal on the backplane.

The Gain Data values that are used by the PMI are NOT mapped to the UDC module's dual port registers. The gain values are held in local tunables with reserved names which must be defined in the UDC task for the drive (A or B). The programmer must use the pre-assigned local tunable reserved names described in Appendix B of this manual.

Note that register values are generally in the appropriate engineering units and that the variable names provided here are suggestions only; your variable names may be different. Duplicate common variable names are not permitted within any one rack.

Table 3.1 lists the configuration views in the AutoMax Programming Executive, the registers to be configured in each, and the section of this instruction manual in which the registers are discussed.

Table 3.2 lists the UDC dual port registers in numerical order.

Note: Any register/bit specific to a particular product type or regulator will be noted as such in the register/bit descriptions.

Register Reference Conventions in this Chapter

Register numbers will be shown using the following convention: X/Y, where X is the drive A register number and Y is the drive B register number. Note that the Interrupt Status Control registers and the Application registers are the same for both drive A and drive B.

Most register/bit descriptions are shown in the following format:

Register Number for Drive A/B Register Name

Bit: The specific bit location, where applicable

Hex Value: The hexadecimal equivalent of the bit number

Range: The upper and lower limits of the register value, where applicable. For bit descriptions, this field will contain N/A.

Access: The level of access by the application task (e.g., Read/Write).

UDC Error Code: A drive fault's corresponding error code. This is reported in the log for the task in which the error occurred.

LED: The corresponding faceplate LED, where applicable.

Description: A description of the register or bit.

View	Register Range	Described in Section:
Port 0	Drive A: 0-5 Drive B: 12-17	3.1
Port 1	Drive A: 6-11 Drive B: 18-23	3.1
Command Registers	Drive A: 100-107 Drive B: 1100-1107	3.3
Feedback Registers	Drive A: 200-221 Drive B: 1200-1221	3.4
Application Registers Updated Every Scan	300-599	3.5
Application Registers Updated Every Nth Scan	1300-1599	3.5
UDC Module Test I/O Registers	1000-1017	3.6
ISCR Data Registers	2000-2001	3.7

Table 3.1 - UDC Module Configuration Views and Registers

Registers	Function	
0-23	Rail I/O port registers	
24-79	System Use Only	
80-89	UDC/PMI communication status registers for drive A (monitor only)	
90-99	System Use Only	
100-107	Command registers for drive A	
108-199	System Use Only	
200-221	Feedback registers for drive A	
222-299	System Use Only	
300-599	Application registers updated every scan for drives A and B	
600-999	System Use Only	
1000	UDC module test switch register	
1001-1017	UDC module meter port setup registers	
1018-1079	System Use Only	
1080-1089	UDC/PMI communication status registers for drive B (monitor only)	
1090-1099	System Use Only	
1100-1107	Command registers for drive B	
1108-1199	System Use Only	
1200-1221	Feedback registers for drive B	
1222-1299	System Use Only	
1300-1599	Application registers updated every Nth scan for drives A and B	
1600-1999	System Use Only	
2000-2010	Interrupt Status and Control registers for drives A and B	
2011-2047	System Use Only	

Table 3.2 - UDC Module Dual Port Memory Register Organization

3.1 Rail I/O Port Registers (Registers 0-23)

The Rail I/O Port 0 and Port 1 views are used to assign variable names to the rail ports on the PMI. If you have no hardware attached to these ports, you do not configure these registers. All of the Rail data for PMI A and PMI B is combined into one section of the dual port memory. Refer to Table 3.3. Note that the usage of each register is a function of what type of Rall Is configured. After a Stop All, outputs are reset to zero and inputs continue to be updated.

The appropriate variable configuration screen will be displayed based on the hardware that you have specified to be connected to the port.

The following types of hardware can be connected to these ports. The instruction manual for the hardware shown is in parentheses.

- M/N 45C001 Digital I/O Rail (J-3012)
- M/N 45C630 4-Decade Thumbwheel Switch Input Module (J-3654)
- M/N 45C631 4-Digit LED Output Module (J-3655)
- M/N 61C345 4-Channel Analog Current Input Rail (J-3689)
- M/N 61C346 4-Channel Analog Voltage Input Rail (J-3688)
- M/N 61C350 2-Channel Analog Voltage Input/Output Rail (J-3672)
- M/N 61C351 2-Channel Analog Current Input/Output Rail (J-3673)
- M/N 61C365 4-Channel Analog Current Output Rall (J-3694)
- M/N 61C366 4-Channel Analog Voltage Output Rail (J-3695)

Each Rail I/O port has a set of bits that display any errors that may occur and a fault counter that is incremented each time a bad communication check bit is detected. The user's application program must regularly examine these bits and registers. Refer to Tables 3.4, 3.5, and 3.6. The check bit fault counter is reset to zero when a warning reset signal (register 100/1100) is generated through the UDC module from the application program.

ai		1	B	Rail Type and Signal		
Drive A Registers	Drive B Registers	Drive B Registers Port and Channel	4 Output ¹	4 Input ²	2 Input ³ 2 Output	Digital I/O ⁴
0	12	Port 0 - Channel 0	Output 0	Input 0	Output 0	Digital
1	13	Port 0 - Channel 1	Output 1	Input 1	Output 1	N/A
2	14	Port 0 - Channel 2	Output 2	Input 2	Input 2	N/A
3	15	Port 0 - Channel 3	Output 3	Input 3	Input 3	N/A
4	16	Port 0 - Fault Register (Tables	3.4-3.6)			
5	17	Port 0 - Check Bit Fault Counter Register (Tables 3.4-3.6)				
6	18	Port 1 - Channel 0	Output 0	Input 0	Output 0	Digital
7	19	Port 1 - Channel 1	Output 1	Input 1	Output 1	N/A
8	20	Port 1 - Channel 2	Output 2	Input 2	Input 2	N/A
9	21	Part 1 - Chennel S	Output 3	Input 3	Input 3	N/A
10	22	Port 1 - Fault Register (Tables 3.4-3.6)				
11	23	Part 1 - Check Bit Fault Counter Register (Tables 3.4-3.6)				

Table 3.3 - Rail I/O Port Registers

(1) 4-Output Analog Reil Module (M/N 61C365, 61C366)

(2) 4 Input Analog Rail Module (M/N 61C345, 61C346)

(3) 2-Output/2 Japut Analog Pail Module (M/N 61C350, 61C351)

(4) Digital (4) Pail (M/N 45C1), Thumbwheel Switch Input Module (M/N 45C630), or LED Dusput Module (M/N 45C631)

Drive A Registers	Drive B Registers	Description	
4	16	Port 0 Fault Register	
10	22	Port 1 Fault Register	
		Bit 8: No device plugged into a configured port	
		Bit 9: Bad ID code: device other than a rail is plugged into the port	
		Bit 10: Bad rail communication check bits received	
		Bit 11: PMI interface is not ready	
5	17	Port 0 Check Bit Fault Counter Register	
11 23	Port 1 Check Bit Fault Counter Register		
		The register can be resat by setting bit 9 of the Warning Reset register (100/1100)	

Table 3.4 - Fault Register and Check Bit Fault Counter Register Usage lor a Digital I/O Rail or 4-Output Analog Rail Module

Table 3.5 - Fault Register and Check Bit Fault Counter Register Usage for a 4-Input Analog Rail Module

Drive A Registers	Drive B Registers	Description
4	16	Port 0 Fault Register
10	22	Port 1 Fault Register
		Bit 0: Analog Channel 0 Input Over-Renge
		Bit 1: Analog Channel 0 Input Under-Range
		Bit 2: Analog Channel 1 Input Over-Range
		Bit 3: Analog Channel 1 Input Under-Range
		Bit 4: Analog Channel 2 Input Over-Range
		Bit 5: Analog Channel 2 Input Under-Range
		Bit 6: Analog Channel 3 Input Over-Range
		Bit 7: Analog Channel 3 Input Under-Range
		Bit 8: No device plugged into a configured port
		Bit 9: Bad ID code: device other than a rail is plugged into the port
		Bit 10: Bad rail communication check bits received
		Bit 11: PMI interface is not ready
5	17	Port 0 Check Bit Fault Counter Register
11	23	Port 1 Check Bit Fault Counter Register
		The register can be reset by setting bit 9 of the Warning Reset register (100/1100)

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Drive A Registers	Drive B Registers	Description
4	16	Port 0 Fault Register
10	22	Port 1 Fault Register
		Bit 4: Analog Channel 2 Input Over-Range
		Bit 5: Analog Channel 2 Input Under-Range
		Bit 6: Analog Channel 3 Input Over-Range
		Bit 7: Analog Channel 3 Input Under-Range
		Bit 8: No device plugged into a configured port
		Bit 9: Bad ID code: device other than a rail is plugged into the port
		Bit 10: PMI interface is not ready
~~		Bit 11: Bad rail communication check bits received
5	17	Port 0 Check Bit Fault Counter Register
11	23	Port 1 Check Bit Fault Counter Register
		The register can be reset by setting bit 9 of the Warning Reset register (100/1100)

Table 3.6 - Fault Register and Check Bit Fault Counter Register Usage for a 2-Output/2-Input Analog Rail Module

3.2 UDC/PMI Communication Status Registers (Registers 80-89/1080-1089)

The UDC/PMI Communication Registers display the status of the fiber-optic communications between the UDC module and the PMI. Two consecutive errors will be indicated by a communication fault and the drive will stop. Refer to register 202/1202, bit 15 for more information. Note that the communication status registers are for system use only and can only be monitored. They cannot be defined during configuration for access within the application task. The status of these registers will be retained after a Stop All.

80/1080 UDC Module Ports A/B Status Register

The UDC Module Ports A/B Status register contains bits which describe any errors or warnings reported on the UDC module related to UDC/PMI communication on Port A and Port B. These bits are latched when set and will remain set until a fault reset or warning reset is issued.

Bit: 0 Hex Value: 0001H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Invalid Receive Interrupt bit is set when the interrupt generated by the Universal Serial Controller (USC) is not properly marked.

80/1080 UDC Module Ports A/B Status Register (Continued) Bit: 1 Hex Value: 0002H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The No End of Frame Status Received bit is set if the USC does not report an End of Frame condition when the receive interrupt is generated. Bit: 2 Hex Value: 0004H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The CRC/Framing Error bit is set when the USC reports a CRC or Framing error on the last frame (message) received, Bit: 3 Hex Value: 0008H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Overrun Error bit is set when the USC reports a receive first-in, first-out overrun. Bit: 4 Hex Value: 0010H Sug. Var. Name: N/A Range: N/A :25 Access: Read only UDC Error Code: N/A LED: N/A Description: The DMA Format Error bit is set if the length of the received message does not match the length encoded in the message itself. Bit: 5 Hex Value: 0020H Sug. Ver. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Transmitter Underrun bit is set when the USC reports a transmit first-in, first-out underrun.

80/1080	UDC Module Ports A/B Status Register (Continued)
Bit: 6 Hex Value Sug. Var. Range: N/ Access: R UDC Erro LED: N/A Descriptio counter tic	e: 0040H Name: N/A /A Read only r Code: N/A on: The CCLK Communication Synchronization Error bit is set when two or more CCLK :ks occur and no message is received.
Bit: 7 Hex Value Sug. Var. Range: N/ Access: R UDC Erro LED: N/A Descriptio transmit m after a rese	e: 0080H Name: N/A /A lead only r Code : N/A on: The External Loopback Data Error bit is set during the UDC module loopback test if the nessage does not match the receive message. This test is performed only at power up or et.
Bit: 8 Hex Value Sug. Var. I Range: N/ Access: R UDC Errol LED: N/A Descriptic memory w	:: 0100H Name: N/A /A Read only r Code: N/A on: The Missed Gains bit is set if gain data from the PMI could not be written because /as being written to when the gain values were received.
Bit: 9 Hex Value Sug. Var. i Range: N/ Access: R UDC Erroi LED: N/A Descriptic command.	:: 0200H Name: N/A /A lead only r Code: N/A on: The Multiplexed Data Verification Failure bit is set it data which is muiliplexed into feedback messages does not verify correctly.
Bit: 10 Hex Value Sug. Var. I Range: N/ Access: R UDC Errou LED: N/A Descriptic system is r system. Th module an	e: 0400H Name: N/A A tead only r Code: N/A on: The No Matching PMI Operating System Present bit is set if the correct PMI operating not present in the UDC module's operating system and the PMI is requesting an operating his condition will cause the loading of the PMI operating system to fail; however, the UDC ad the PMI will continue to retry loading the PMI operating system.
80/1080	UDC Module Ports A/B Status Register (Continued)
---	--
Bil: 11	
Hex Value	: 0800H
Sug. Var. 1	Vame: N/A
Range: N/	A
Access: R	ead only
UDC Error	r Code: N/A
LED: N/A	
Description valid PMI of condition withe PMI will	In: The Invalid PMI Operating System Header bit is set if the UDC module cannot locate a operating system header when attempting to load an operating system to a PMI. This will cause the loading of the PMI operating system to fail; however, the UDC module and II continue to retry loading the PMI operating system.
Bit: 12	
Hex Value	· 1000H
Sun Var I	Vame: N/A
Bange: N/	A
Access: A	ead only
UDC Error	Code: N/A
LED: N/A	
Descriptio	n: The Incompatible PMI Hardware bill is set if the PMI hardware is not compatible with the
Pivil operat	ing systems in the ODC operating system.
81/1081	UDC Module Ports A/B Receive Count Register
Hex Value:	: N/A
Sug. Var. N	Name: N/A
Range: N//	A
Access: R	ead only
UDC Error	Cade: N/A
LED: N/A	
Descriptio and Port B.	n: This register contains the number of messages received by the UDC module on Port A . This is a 16-bit value that rolls over when it reaches its meximum.
82/1082	UDC Module Ports A/B CRC Error Count Register
Her Value	• N/A
Suc Var N	Jame: N/A
Banne: Mo	4
Accese B	ead only
UDC Error	Code: N/A
LED: N/A	
Descriptio	n. This register contains the number of mossoors with CBC errors received by the LIDC
module on	Port A and Port B.
83/1083	UDC Module Ports A/B Format Error Count Register
Hex Value:	: N/A
Sug. Var. N	lame: N/A
Range: N//	4
Access: Re	sad only
UDC Error	Code: N/A
LED: N/A	
	ny This register contains the number of measures with formal annual state to the USO

84/1084	PMI A/B Status Register
The PMI A/ related to L remain set	B Status register contains bits which describe any errors or warnings reported by the PMI JDC/PMI communication on PMI A and PMI B. These bits are latched when set and will until a fault reset or warning reset is issued.
Bit: 0 Hex Value: Sug. Var. N Range: N/A Access: Re UDC Error LED: N/A Description Serial Cont	: 0001H Jame: N/A A aad only Code: N/A :: The Invalid Receive Interrupt bit is set when the interrupt generated by the Universal roller (USC) is not properly marked.
Bit: 1 Hex Value: Sug. Var. N Range: N/A Access: Re UDC Error LED: N/A Description Frame cont	0002H Iame: N/A A sad only Code: N/A n: The No End of Frame Status Received bit is set if the USC does not report an End of dition when the receive interrupt is generated.
Bit: 2 Hex Value: Sug. Var. N Range: N/A Access: Re UDC Error LED: N/A Description last frame (i	0004H l ame: N/A aad only Code: N/A n: The CRC/Framing Error bit is set when the USC reports a CRC or Framing error on the message) received.
Bit: 3 Hex Value: Sug. Var. N Range: N/A Access: Re UDC Error LED: N/A Description	0006H ame: N/A ad only Code: N/A n: T he Overrun Error bit is set when the USC reports a receive first-in, first-out overrun.
Bit: 4 Hex Value: Sug. Var. N Range: N/A Access: Re UDC Error LED: N/A Description the length e	0010H lame: N/A A ad only Code: N/A n: The DMA Format Error bit is set if the length of the received message does not match encoded in the message itself.

84/1084 PMI A/B Status Register (Continued) Bit: 5 Hex Value: 0020H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Transmitter Underrun bit is set when the USC reports a transmit first-in, first-out underrun. Bit: 6 Hex Value: 0040H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The CCLK Communication Synchronization Error bit is set when two or more CCLK counter ticks occur and no message is received. Bit: 8 Hex Value: 0100H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: LED: N/A Description: The UDC CCLK Communication Synchronization Error bit is set if two UDC CCLK ticks occur and no message is received from the PMI. Bit: 9 Hex Value: 0200H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Multiplexed Data Verification Failure bit is set if data multiplexed into command/feedback messages does not verify. Bil: 12 Hex Value: 1000H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Invalid PMI Start Operating System Address bit is set by the PMI if the operating system is not within the allocated operating system address area. This condition will cause the loading of the PMI operating system to fail; however, the UDC module and the PMI will continue to retry loading the PMI operating system.

	PMI A/B Status Register (Continued)
88-12	
Hey Velu	e: 2000H
Sun Var	Name: N/A
Banna: M	Παιτία: 370 (Δ
Accore-	
HDC Erro	e Code: N/A
LED NIA	
Descripti	en: The incutificient BMI Memory in Lond the BMI Commission Contains hit is not by the DMI V.
bescripu	on: The insultcient Pivil Memory to Load the Pivil Uperating System bit is set by the Pivil if
there is in	sufficient memory for loading the operating system. This condition will cause the loading of
the PMIC	perating system to fail, nowever, the upp module and the PMI will continue to retry loading
the FMI O	peraung system.
Bit: 14	
Hex Value	a: 4000H
Sug. Var.	Name: N/A
Range: N	/A
Access:	Bead only
UDC Em	r Code: N/A
IED. NVA	i ooda nija
Deperioti	nes The level of DML and Address bit is set by the DML (the address studiet if is to be d
Descripti	bit: The invalid Pivil Load Acoress bit is set by the Pivil in the address at which it is to ided
the opera	ting system is invalid. This condition will cause the loading of the PMI operating system to
Tail; nowe	ver, the ODC module and the PMI will continue to relay loading the PMI operating system.
Bit: 15	
Hex Value	e: 8000H
Sug. Var.	Name: N/A
Range: N	/A
Access F	Reari onlu
HOC Erro	r Code: N/A
LED: N/A	I COUR. N/A
Depariati	en. The DMI Operation Contem Operflow into Operal Manager, bit is easily the DMI Kills
Description	on: The Pivil Operating System Overnow into Stack memory bit is set by the Pivil it the
loading bi	the PNII operating system will overrun the PMI stack memory area. This condition will
cause me	Inspling of the PML onersping system to fair however they like module and the PML will
	Totaling of the film operating system to fair, now ever, the observations and the film min
conuncer	o retry loading the PMI operating system.
85/1085	PMI A/B Receive Count Register
85/1085 Hex Value	PMI A/B Receive Count Register
85/1085 Hex Value Sug Ver	PMI A/B Receive Count Register
85/1085 Hex Value Sug. Var.	PMI A/B Receive Count Register is: N/A Name: N/A
85/1085 Hex Value Sug. Var. Range: N	PMI A/B Receive Count Register a: N/A Name: N/A /A
85/1085 Hex Value Sug. Var. Range: N Access: F	PMI A/B Receive Count Register >: N/A Name: N/A A Read only Particle in the postaling system.
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A A Read only r Code: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A A Read only r Code: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A A Read only r Code: N/A on: The PMI A/B Receive Count register contains the number of messages received by the
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar	PMI A/B Receive Count Register a: N/A Name: N/A /A Read only r Code: N/A con: The PMI A/B Receive Count register contains the number of messages received by the ind Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum.
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086	PMI A/B Receive Count Register contains the number of messages received by the or The PMI A/B Receive Count register contains the number of messages received by the id Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum.
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086	PMI A/B Receive Count Register contains the number of messages received by the id Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum.
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A Name: N/A Name: N/A Name: N/A PMI A/B Receive Count register contains the number of messages received by the Ind Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum. PMI: A/B CRC Error Count Register a: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value	PMI A/B Receive Count Register a: N/A Name: N/A A Read only r Code: N/A on: The PMI A/B Receive Count register contains the number of messages received by the id Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum. PMI A/B CRC Error Count Register a: N/A Name: N/A Name: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value Sug. Var. Range: N	PMI A/B Receive Count Register a: N/A Name: N/A A A A A A A A A A A A A A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value Sug. Var. Range: N Access: F	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A Name: N/A Name: N/A con: The PMI A/B Receive Count register contains the number of messages received by the id Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum. PMI: A/B CRC Error Count Register a: N/A Name: N/A Name: N/A Name: N/A Name: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value Sug. Var. Range: N Access: F UDC Erro	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A Name: N/A con: The PMI A/B Receive Count register contains the number of messages received by the id Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum. PMI A/B CRC Error Count Register a: N/A Name: N/A Name: N/A Name: N/A Name: N/A Name: N/A Name: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A Name: N/A Name: N/A Name: N/A con: The PMI A/B Receive Count register contains the number of messages received by the id Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum. PMI: A/B CRC Error Count Register e: N/A Name: N/A Name: N/A Name: N/A Name: N/A Name: N/A
85/1085 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio Drive A ar 86/1086 Hex Value Sug. Var. Range: N Access: F UDC Erro LED: N/A Descriptio	PMI A/B Receive Count Register a: N/A Name: N/A Name: N/A Need only r Code: N/A con: The PMI A/B Receive Count register contains the number of messages received by the ind Drive B PMIs. This is a 16-bit value that rolls over when it reaches its maximum. PMI: A/B CRC Error Count Register e: N/A Name: N/A

87/1087 PMI A/B Format Error Count Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: This register contains the number of messages with format errors received by the Drive A and Drive B PMIs.

88/1088 UDC Module Ports A/B Fiber-Optic Link Status Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A

Description: This register indicates the current operating state of liber-optic links A and B. The lower byte (bits 0-7) indicates the actual link status while the upper byte (bits 8-15) shows whether the communication taking place is synchronized or not.

- If the lower byte is equal to (xx01H), the UDC module is waiting for a request from the PMI for an operating system.
- If the lower byte is equal to (xx02H), the UDC module is downloading an operating system to the PMI.
- If the lower byte is equal to (xx03H), the UDC module and the PMI are exchanging data.
- If the lower byte is equal to (xx06H), the external loopback test is being conducted on the fiber-optic link.
- If the upper byte is equal to (01xxH), the communication between the UDC module and the PMI is synchronized.
- If the upper byte is equal to (02xxH), the communication between the UDC module and the PMI is unsynchronized.

89/1089 UDC Module Ports A/B Transmitted Message Count Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: This register contains the number of messages transmitted by the UDC module on Port A and Port B.

3.3 Command Registers (Registers 100-199/1100-1199)

The Command Registers view is used to configure command registers. These registers are used for command data sent to the PMI by the UDC module at the end of every scan of the UDC Processor. Note that the bits in these registers (except bit 15 in register 100/1100) are used to command action only and do not indicate the status of the action commanded. The feedback registers (registers 200/1200 to 299/1299) are provided for this purpose. The status of the command registers is not relained after a Stop All.

100/1100 Drive Control Register

The Drive Control register contains the bits that control the operation of the drive. The SA3000 drive can operate in one of four modes: idle, torque minor loop run, PMI tuning, and bridge test. The default operating mode is idle; the other three modes are selected in the Drive Control register. (Each of these modes is described in detail in the SA3000 Diagnostics, Troubleshooting, and Start-Up Guidelines instruction manual.)

All bits in this register (except bit 15) can only be written to by a task on an AutoMax Processor; they cannot be written to by a task on a UDC module. All read/write bits in this register are edge-sensitive and must be maintained in order to assert the command.

Bh: 0

Hex Value: 0001H Sug. Var. Name: TRQ_RUN@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The Torque Run Enable bit is set to enable the minor loop in the PMI Processor.

Bit: 1

Hex Value: 0002H Sug. Var. Name: PMI_TUN@ Range: N/A Access: Read/Write UDC Error Code: N/A

LED: N/A

Description: The Enable Tuning bit is set to request the PMI Processor to calculate the values for local tunables STATOR_R_E4% (stator resistance), STATOR_T_E4% (stator time constant), and STATOR_IZ_E1% (no load stator current). When the PMI Processor completes the calculations, it sets bit 1 in register 200/1200.

Bit: 2

Hex Value: 0004H Sug. Var. Name: BRG_TST@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The Bridge Test Enable bit is set to enable the bridge test. The bridge test turns on individual or sets of power devices in the Power Mocule and is used to verify the gate cable connections and power devices. This test is normally performed at the factory and should not need to be performed again unless the power devices are replaced. Note that the motor must be disconnected before this test is run or equipment damage may result. Refer to the SA3000 Drive Diagnostics, Troubleshooting, and Start-Up Guidelines instruction manual for more information about the bridge test.

The value in the Bridge Test Code register (105/1105) is used to select which power device to turn on. When Power Modules are connected in parallel, bits 10, 11, and 12 in this register are used to select which Power Module to test.

100/1100 Drive Control Register (Continued) Bit: 4 Hex Value: 0010H Sug. Var. Name: BUS ENA@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The Bus Enable bit is set to request the PMI Processor to close the pre-charge contactor. When bus voltage is greater than the value in the under voltage threshold tunable variable (UVT_E0%) and has reached a steady state, and feedback indicates that the pre-charge contector has closed, the PMI Processor will set bit 4 of register 200/1200 (D-C Bus Ready). Refer to the appropriate SA3000 Power Modules manual for more information about internal D-C bus control. Bit: 6 Hex Value: 0040H Sug. Var. Name: VOA REQ@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: For SA3000 Parallel Inverter applications, PMI B's vector orientation must be aligned with PMI A before the torque loop is enabled. The application task sets the Vector Orientation Alignment Request bit in register 1100 to enable PMI B to align its vector orientation with that of PMI A. This bit is used only when SA3000 Parallel Invertors has been selected during UDC module. configuration. Refer to section 4.2.4 and Appendix C for more information about \$A3000 Parallel Inverters. Blt: 8 Hex Value: 0100H Sug. Var. Name: FLT RST@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The Fault Reset bit is set and reset to clear the Drive Fault register 202/1202. After a drive fault is latched, the Drive Fault register must be cleared before the drive can be re-started. First, any command bits that have been set in the Drive Control register (100/1100) must be turned off. Once the cause of the fault has been corrected, the Fault Reset bit must be sumed on and then off again. The Fault Reset bit will clear the entire Drive Fault register. Then the desired command bits may be turned on again. The Fault Reset bit is edge-sensitive, i.e., leaving it set will not clear the fault register continuously. Note that if the fault condition still exists after register 202/1202 is cleared, it will continue to moder drive faults until the problem has been corrected. 81: 9 Hex Value: 0200H Sug. Var. Name: WRN RST@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The Warning Reset bit is set and reset to clear the Drive Warning register 203/1203. This bit is edge-sensitive, i.e., leaving it set will not clear the warning register continuously. Bit: 10 Hex Value: 0400H Sug. Var. Name: PPM ENA@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: When Power Modules are connected in parallel, the Enable Parellel Power Module A bit is set to select Power Module A for the bridge test. The system reads the status of this bit only onco after the bridge test is enabled.

100/1100 Drive Control Register (Continued) Bit: 11 Hex Value: 0800H Sug. Var. Name: PPM ENB@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: When Power Modules are connected in parallel, the Enable Parallel Power Module B bit is set to select Power Module B for the bridge test. The system reads the status of this bit only once after the bridge test is enabled. Bit: 12 Hex Value: 1000H Sug. Var. Name: PPM ENC@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: When Power Modules are connected in parallel, the Enable Parallel Power Module C bit is set to select Power Module C for the bridge test. The system reads the status of this bit only once after the bridge test is enabled. Bit: 15 Hex Value: 8000H Sug. Var. Name: UDC RUN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The UDC Task Running bit is a status bit that indicates that the UDC task is running. This bit is used by the PMI Processor to prevent the minor loop from running if the UDC task is not running. This bit must NOT be written to by the user. This is a status bit that must only be written to by the operating system. 101/1101 I/O Control Register The I/O Control Register contains the bits that control the I/O on the Resolver & Drive I/O module and the operation of the resolver strobe. Bit: 2 Hex Value: COC4H Sug. Var. Name: EXT LED Range: N/A Access: Read/Write UDC Error Code: N/A LED: EXT FLT LED on the PMI Processor module Description: The External Fault LED bit is set by the application task to turn on the EXT FLT LED on the PMI Processor module. Bit 4 Hex Value: 0010H Sug. Var. Name: AUX OUT@. Range: N/A Access: Read/Write UDC Error Code: N/A LED: AUX OUT LED on the Resolver & Drive I/O module Description: The Auxiliary Output bit is set to turn on the auxiliary output on the Resolver & Drive I/O module.

101/1101 I/O Control Register (Continued)

Bit: 6

Hex Value: 0040H Sug. Var. Name: RES_CAL@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The Enable Resolver Calibration Test bit is set to start the test that determines the resolver's balance value. This value will be stored in the pre-defined local tunable RES_BAL%. This bit is edge-sensitive. The lest will turn off if the bit is reset. Refer to register 201/1201, bits 6 and 7 for

Power Module Interface Rack instruction manual for additional resolver calibration information.

Bit: 8 Hex Value: 0100H Sug. Var. Name: STR_ENA@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The Enable External Strobe bit is set to enable the external strobe on the resolver to capture the position of the resolver when the rising edge of the external strobe is detected. As long as this bit is set, the external strobe is enabled. If this bit is set in conjunction with bit 9, the resolver position is captured on both the rising and falling edges of the input signal. See register 201/1201, bits 8 and 9 for additional information. The resolver position data is placed in the Resolver Strobe Position register (register 216/1216).

information on the calibration test complete bits. Refer to the Distributed Power System SA3000

Bit: 9

Hex Value: 0200H Sug. Var. Name: STH_ENF@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The Enable External Strobe Falling Edge bit is set to enable the external strobe on the resolver to capture the position of the resolver when the falling edge of the external strobe is detected. As long as this bit is set, the external strobe is enabled. If this bit is set in conjunction with bit 8, the resolver position is captured on both the rising and falling edges of the input signal. See register 201/1201, bits 8 and 9 for additional information. The resolver position data is placed in the Resolver Strobe Position register (register 216/1216).

Bit: 10

Hax Value: 0400H Sug. Var. Name: TUNE_IZ@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The Enable STAT

Description: The Enable STATOR_IZ_E1% Tuning bit is set to start the procedure to tune the value In STATOR_IZ_E1%. Note that this procedure is used in constant power applications only. Refer to Appendix B for more information on this procedure. For SA3000 Parallet Inverters, this procedure should be performed in drive A and the result copied to drive B.

101/1101 I/O Control Register (Continued)

Bit: 15 Hex Value: 8000H Sug. Var. Name: UDC_LB@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The UDC Module External Loopback bit is set to enable the external loopback test on the UDC module's fiber-optic ports. Register 101, bit 15 controls the COMM A test while register 1101, bit 15 controls the COMM B test. Note that this bit must be set to 0 before the loopback connector is removed from the UDC module's fiber-optic ports. Refer to the Fiber-Optic Cabling instruction manual for additional information.

102/1102 Torque Reference Register

Hex Value: N/A

Sug. Var. Name: TRO_REF% Range: -4095 to +4095 (full scale torque in either direction) Access: Read/Write UDC Error Code: N/A LED: N/A Description: The value in the Turque Reference repiritor in the r

Description: The value in the Torque Reference register is the reference sent to the PMI Processor for use in the minor loop. This value corresponds to the torque produced by the configured maximum motor current (rated motor torque x motor overload ratio). The value in this register is limited to not exceed +/- 4095. See register 203/1203, bit 4 for more information.

104/1104 Flux Reference Register or Jd Reference Register

Hex Value: N/A Sug. Var. Name: FLX_REF% or ID_REF% Range: 0 to 4095 Access: Read/Write UDC Error Code: N/A LED: N/A

Description: If SA3000 Vector or SA3000 Vector with Constant Power is selected during UDC module configuration, register 104/1104 is used as the Flux Reference register (FLX_REF%). The value in the Flux Reference register defines the ratio used to scale the value for magnetizing current (STATOR_IZ_E1%) when the Enable UDC Flux Reference option has been selected during parameter entry for the SA3000 Vector regulator, or the Manual Compensation option has been selected for the SA3000 Vector with Constant Power regulator. For example, if register 104=4095, then the full value of STATOR_IZ_E1% will be used for magnetizing current.

If SA3000 Parallel Inverters is selected during UDC module configuration, register 1104 is used as the Id Reference register for PMI B. The drive B UDC task must copy the Id reference value calculated by PMI A (see register 217, Id Feedback) into register 1104. Refer to section 4.2.4 and Appendix C for more information about SA3000 Parallel Inverters.

105/1105 Bridge Test Code Register

Hex Value: N/A Sug. Var. Name: TST_CODE% Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The value written to the Bridge Test Code register determines which power device to turn on during the bridge test. The six least significant bits correspond to the six power devices.

Bit 0UUpper Power DeviceBit 1VUpper Power DeviceBit 2WUpper Power DeviceBit 3ULower Power DeviceBit 4VLower Power DeviceBit 5WLower Power Device

Patterns that turn on the same device in the upper and lower bridge are not accepted, and no device will be turned on. Bit 4 in the Drive Warning register (203/1203) is set if an illegal pattern is used.

When a value of -1 is entered in this register, the test will cycle through each power device individually in the following order: U-, U+, V , V+, W-, W-. On the High Power A-C Power Modules, the corresponding LEDs will turn on.

When Power Modules are connected in parallel, bits 10, 11, and 12 in the Drive Control register (100/1100) are used to select the Power Module to be tested.

Refer to the SA3000 Diagnostics, Troubleshooting, and Start-Up Guidelines for more information about the bridge test.

106/1106 PMI D/A Output Register

Hex Value: N/A Sug. Var. Name: PMI_DA% Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A

Description: The value in the PMI D/A Output register is transmitted to the PMI Processor at the end of every UDC task scan. Note that a task must copy the desired value into this register. The value can then be displayed on one of the four PMI Processor meter ports. This register can contain any variable in the AutoMax system as long as it is a 16-bit integer. Double-integer or floating point values cannot be displayed on the PMI Processor's D/A meter ports.

107/1107 Vector Orientation Reference Register

Hex Value: N/A Sug. Var. Name: VO_REF% Range: 0 to 4095 Access: Read/Write UDC Error Code: N/A LED: N/A

Description: For SA3000 Parallel Inverters applications, register 1107 is used as PMI B's Vector Orientation Reference register. This register contains the commanded phase angle value copied by the drive B UDC task from PMI A (see register 218, Vector Orientation Feedback). PMI B compares the PMI A phase angle to its own commanded phase angle and adjusts the PMI B phase angle, if necessary, to align the two. Refer to section 4.2.4 and Appendix C for more information on SA3000 Parallet Inverters. This register is used only if SA3000 Parallel Inverters is selected during UDC module configuration.

3.4 Feedback Registers (Registers 200-299, 1200-1299)

The Feedback Registers view is used to configure the feedback registers that display the current status of the drive. These registers are updated by the PMI Processor and sent to the UDC module over the fiber-optic link before every scan of the UDC task. The status of these registers is retained after a Stop All.

200/1200 Drive Status Register

The bits in the Drive Status register indicate the current state of the drive. The bits reflect the status of the activity initiated through the Drive Control register (register 100/1100).

```
Bil: 0
Hex Value: 0001H
Sug. Var. Name: TRQ_ON@
Range: N/A
Access: Read only
UDC Error Code: N/A
LED: N/A
Description: The PMI Processor sets the Torque Control On bit in response to the TRQ_RUN@
command after all of the interlock tests are passed to indicate that the minor loop is running and the
motor is energized.
Bit: 1
Hex Value: 0002H
Sug. Var. Name: PMI ATC@
Range: N/A
Access: Read only
UDC Error Code: N/A
LED: N/A
Description: The PMI Processor sets the Automatic Tuning Complete bit in response to the
PMI_TUN@ command to indicate it has completed the calculations for local tunables
STATOR_R_E4% (stator resistance), STATOR_T_E4% (stator time constant), and STATOR_IZ_E1%
(no load stator current). Refer to Appendix B for more information on these local tunables.
Bil: 2
Hex Value: 0004H
Sug. Var. Name: TRF SP@
Range: N/A
Access: Read only
UDC Error Code: N/A
LED: N/A
Description: The Torque Reference Saturation Plus bit is set when the system is requesting
maximum positive torque from the drive.
Bit: 3
Hex Value: 0010H
Sug. Var. Name: TRF SM@
Range: N/A
Access: Read only
UDC Error Code: N/A
LED: N/A
Description: The Torque Reference Saturation Minus bit is set when the system is requesting
maximum negative torque from the drive.
```

200/1200 Drive Status Register (Continued) Bit A Hex Value: 0010H Sug. Var. Name: BUS RDY@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The PMI Processor sets the D-C Bus is Ready bit in response to the BUS_ENA@ command when it detects D C bus voltage is greater than the under voltage threshold value stored in local tunable UVT_E0% and has reached a steady state, and foodback indicates that the pre-charge contactor has closed. Refer to the appropriate SA3000 Power Modules manual for more information about internal D-C bus control. Bir 5 Hex Value: 0020H Sug. Var. Name: PWR RNG@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: If the drive has been configured during parameter entry to operate in the constant power range, the PMI Processor will set the Constant Power Region bit to 1 when the drive is operating in the constant power region (flux weakening occurs). BIT: 6 Hex Value: 0040H Sug. Var. Name: VOA OK@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: PMI B sets the Vector Orientation Alignment OK bit in response to VOA REQ@ (register 100/1100, bit 6) when vector alignment is completed. If the phase error between PMLA and PMLB is greater than 5 degrees after alignment, VOA_OK@ will momentarily turn off, and WAN_VOA@ (203/1203, bit 10) will be latched to indicate that there is an error in alignment. This bit is used only when \$A3000 Parallel Inverters is selected during UDC module configuration. Bil: 8 Hex Value: D100H Sug. Var. Name: FLT@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The PMI Processor sets the Fault Detected bit if a fault occurs (see Drive Fault register 202/1202). It is reset by bit 8 of register 100/1100. Bil- G Hex Value: 0200H Sug. Var. Name: WRN@ Range: N/A Access: Read only

UDC Error Code: N/A LED: N/A Description: The PMI Processor sets the Warning Detected bit if a warning occurs (see Drive Warning register 203/1203). It is reset by bit 9 of register 100/1100.

200/1200 Drive Status Register (Continued)

Bit: 14

Hex Value: 4000H Sug. Var. Name: CCLK_OK@ Range: N/A Access: Read only UDC Error Code: N/A

LED: N/A

LED: N/A

Description: The PMI Processor sets the CCLK Synchronized bit when CCLK in the UDC module is synchronized with CCLK in the PMI Processor. This bit will be equal to zero when CCLK is not turned on in the AutoMax rack or if there have been two consecutive instances when CCLK is not synchronized after you have turned CCLK on. In this case, the feedback data from the PMI is not current.

This bit should normally be used only in the start permissive logic for the drive (which must be true only once to start the drive). It does not have to be used in the run permissive logic for the drive (which must be true during the entire execution of the task).

Note that applications that require vory tight synchronization between the UDC module and the PMI (e.g., positioning applications) may require the use of this bit in the run permissive togic.

Refer also to the Communication Lost fault bit description (register 202/1202, bit 15).

Bit: 15

Hex Value: 8000H Sug. Var. Name: PMI_OK@ Range: N/A Access: Reed only

UDC Error Code: N/A

LED: N/A

Description: The PMI Processor sets the PMI Operating System Loaded bit when the operating system has been successfully downloaded from the UDC module to the PMI Processor after power up.

201/1201 I/O Status Register

The bits in the I/O Status register indicate the current state of the inputs on the Resolver & Drive I/O module.

Bit: 0 Hex Value: 0001H Sug. Var. Name: RPI@ Range: N/A Access: Read only UDC Error Code: N/A LED: RPI on the Resolver & Drive I/O module Description: The Run Permissive Input bit reflects the status of the input signal connected to pin A on the DRIVE I/O connector. When the signal is present, this bit is set. This signal typically originates from the drive's coast stop circuit. Bit: 1 Hex Value: 0002H Sug. Var. Name: M FDBK@ Range: N/A Access: Read only UDC Error Code: N/A LED: AUX IN1 on the Resolver & Drive I/O module Description: The M-Contactor Feedback bit reflects the status of the M-contactor feedback input.

signal which is connected to the AUX IN1 input on the Reseiver & Drive I/O module. When the input signal is present, this bit is set.

201/1201 I/O Status Register (Continued) Bit: 2 Hex Value: 0004H Sug. Var. Name: AUX IN2@ Range: N/A Access: Read only UDC Error Code: N/A LED: AUX IN2 on Resolver & Drive I/O module Description: The Auxiliary Input 2 bit reflects the status of the 115 VAC auxiliary input 2 on the Resolver & Drive I/O module. When the input signal is present, this bit is set, Bit: 3 Hex Value: 0008H Sug. Var. Name: AUX IN3@ Range: N/A Access: Read only UDC Error Code: N/A LED: AUX IN3 on the Resolver & Drive I/O module Description: The Auxiliary Input 3 bit reflects the status of the 115 VAC auxiliary input 3 on the Resolver & Drive I/O module. When the input signal is present, this bit is set. Bit d Hex Value: 0010H Sug. Var. Name: AUX IN4@ Range: N/A Access: Read only UDC Error Code: N/A LED: AUX IN4 on the Resolver & Drive I/O module Description: The Auxiliary Input 4 bit reflects the status of the 115 VAC auxiliary input 4 on the Resolver & Drive I/O module. When the input signal is present, this bit is set. Bit: 5 Hex Value: 0020H Sug. Var. Name: AUX INS@ Range: N/A Access: Read only UDC Error Code: N/A LED: AUX IN5 on the Resolver & Drive I/O module Description: This Auxiliary Input 5 bit reflects the status of the 115 VAC auxiliary input 5 on the Resolver & Drive I/O module. When the input signal is present, this bit is set. Bit 6 Hex Value: 0040H Sug. Var. Name: RES GAN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Resolver Gain Calibrated bit is set when the resolver gain calibration procedure is complete. This procedure is performed when the value stored in local tunable RES_GAN% equals zero. Bil: 7 Hex Value: 0080H Sug. Var. Name: RES BAL@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Resolver Balance Calibrated blt is set when the resolver balance calibration procedure is complete. This procedure is performed when the Enable Resolver Calibration Procedure bit (register 101/1101, bit 6) is set and the motor is turning.

201/1201 I/O Status Register (Continued) Bit: 8 Hex Value: 0100H Sug. Var. Name: STR DET@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The External Strobe Detected bit is set when the external strobe on the motor's resolver is detacted. Register 216/1216 displays the position of the resolver at the time of the strobe. Note that this bit is set for only one scan allowing a shobe to be detected every scan. The UDC task can check the External Strobe Detected bit each scan to ensure the validity of the strobe data in register 216/1216. Bit: 9 Hex Value: 0200H Sug. Var. Name: STR LVL@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The External Strobe Level bit is set or reset by the system when the external strobe is detected. It indicates whether the external strobe level was rising (1) or falling (0). BN: 10 Hex Value: 0400H Sug. Var. Name: TUNED IZ@ Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The STATOR_IZ_E1% Tuning Complete bit is sot to indicate that the system has successfully tuned the value in STATOR_IZ_E1%. Note that this procedure is used in constant power applications only. Refer to Appendix B for more Information on this procedure. 202/1202 Drive Fault Register The bits in the Drive Fault register indicate the cause of a drive shutdown. The bits in this register are latched until they are reset by setting the Fault Reset bit (bit 6) of the Drive Control register (100/1100). Alter turning the Fault Reset bit on, the drive may be re-started after turning the desired command bit off and then back on again. If the fault condition still exists, the identifying bit in this register will immediately be set again. The fault conditions reported in this register result in turning off the drive. The UDC task is not stopped automatically when a drive fault occurs unless it is specifically instructed to in an application task. The user must ensure that the AutoMax application task tests register 202/1202 and takes appropriate action if a fault occurs. Note that the status of this register is also reported in the error log for the task in which the error occurred. Bit: 0 Hex Value: 0001H Sug. Var. Name: FLT OV@ Range: N/A Access: Read only UDC Error Code: 1018 LED: EXT FLT on the PMI Processor module Description: The D-C Bus Over Voltage Fault bit is set when hardware detects D-C bus voltage exceeds 800V for Medium Power A-C Power Modules or 925V for High Power A-C Power Modules. BH: 1 Hex Value: 0002H Sug. Var. Name: FLT DCI@ Range: N/A Access: Read only UDC Error Code: 1020 LED: P.M. FLT on the PMI Processor module Description: The D-C Bus Over Current Fault bit is set if D-C bus current exceeds 125% of the rated Power Module current.

202/1202 Drive Fault Register (Continued) Bit: 2 Hex Value: 0004H Sug. Var. Name: FLT GND Range: N/A Access: Read only UDC Error Code: 1021 LED: EXT FLT on the PMI Processor module Description: The Ground Current Fault bit is set if ground current exceeds the hardware trip point. NOTE: This bit is not used if the PMI Rack contains a version 60023-5 or later A-C Technology module. BIE 3 Hex Value: 0008H Sug. Var. Name: FLT IOC@ Range: N/A Access: Read only UDC Error Code: 1017 LED: P.M. FLT on the PMI Processor module Description: The Instantaneous Over Current Fault bit is set if an over current occurs in one of the power devices. Register 204/1204 bits 0-5 indicate which power device detacted the over current. Bit 6 of register 204/1204 will also be set if the over current was detected in the Intelligent Power Module. When Power Modules are connected in parallel, registers 220/1220 and 221/1221 indicate the status of Power Modules B and C, respectively. Bit: 4 Hex Value: 0010H Sug. Var. Name: FLT LPI@ Range: N/A Access: Read only UDC Error Code: 1022 LED: PM. FLT on the PMI Processor module. Description: The Local Power Interface Fault bit is set if the power supply on the Local Power Interface module located in the Power Module is not within tolerance. Bit: 5 Hex Value: 0020H Sug. Var. Name: FLT GDI@ Range: N/A Access: Read only UDC Error Code: 1023 LED: OK on Gate Driver Interface module Description: The Gate Driver Interface Fault bit is set if the power supply on the Gate Driver Interface (GDI) module is not within tolerance. If Power Modules are connected in parallel, bit 7 in register 204/1204, 220/1220, or 221/1221 is set to indicate which GDI module is affected. Bit: 6 Hex Value: 0040H Sug. Var. Name: FLT CHG@ Range: N/A Access: Read only UDC Error Code: 1024 LED: EXT FLT and P.M. FLT on the PMI Processor module Description: The Charge Bus Time-out Fault bit is set to indicate one of the following conditions: The D-C bus is not fully charged within 10 seconds after the bus enable bit (register 100/1100. bit 4) is set. The drive is on and feedback indicates that the pre-charge contactor has opened. D-C bus voltage is less than the value stored in the Power Loss Fault Threshold (PLT_E0%) tunable variable. If this bit is set, verify that incoming power is at the appropriate level. If the power level is correct, the problem is in the Power Module. If Power Modules are connected in parallel, bit 8 in register 204/1204, 220/1220, or 221/1221 is set to indicate which Power Module is affected.

202/1202 Drive Fault Register (Continued) Bit: 7 Hex Value: 0080H Sug. Var. Name: FLT OT@ Range: N/A Access: Read only UDC Error Code: 1016 LED: P.M. FLT on the PMI Processor module Description: The Over Temperature Fault bit is set if the fault level thermal switch in the Power Module opens. If Power Modules are connected in parallel, bit 12 is set in register 204/1204, 220/1220. or 221/1221 to indicate which Power Module is affected. Bit: 8 Hex Value: 0100H Sug. Var. Name: FLT TBW@ Range: N/A Access: Read only UDC Error Code: 1008 LED: FDBK OK on the Resolver & Drive I/O module Description: The Resolver Broken Wire Fault bit is set if a sine or cosine signal from the resolver is missing due to a broken wire or the resolver gain tunable (RES_GAN%) has been set too low. Bit: 9 Hex Value: 0200H Sug. Var. Name: FLT RES@ Range: N/A Access: Read only UDC Error Code: 1009 LED: N/A Description: The Resolver Fault bit is set if the fuse blows on the Resolver & Drive I/O module. Bit: 10 Hex Value: 0400H Sug. Var. Name: FLT OSP@ Range: N/A Access: Read only UDC Error Code: 1010 LED: EXT FLT on the PMI Processor module Description: The Over Speed Fault bit is set if the motor's speed exceeds the value entered as the Over Speed Trip (RPM) configuration parameter. Bit: 11 Hex Value: 0800H Sug. Var. Name: FLT PTM@ Range: N/A Access: Read only UDC Error Code: 1011 LED: OK on the A-C Power Technology module Description: The Power Technology Fault bit is set to indicate a problem with the A-C Power Technology module, the Local Power Interface (LPI) module in the Power Module or the cable connection between them. Bit 12 Hex Value: 1000H Sug. Var. Name: FLT PS@ Range: N/A Access: Read only UDC Error Code: 1012 LED: PWR OK on the Power Supply module Description: The PMI Power Supply Fault bit is set if the PMI power supply is not working correctly.

202/1202 Drive Fault Register (Continued) Bit: 13 Hex Value: 2000H Sug. Var. Name: FLT BUS@ Range: N/A Access: Read only UDC Error Code: 1013 LED: N/A Description: The PMI Bus Fault bit is set if there is a bus fault in the PMI rack. This is indicated when the Resolver & Drive I/O module and the A-C Power Technology module do not respond to requests from the PMI processor. This error indicates that there is a hardware problem in the rack. Bit: 14 Hex Value: 4000H Sug. Var. Name: FLT RUN@ Range: N/A Access: Read only UDC Error Code: 1014 LED: N/A Description: The UDC Run Fault bit is set if the UDC task stops while the minor loop is running in the PMI Processor. BIt: 15 Hex Value: 8000H Sug. Var. Name: FLT COM@ Range: N/A Access: Read only UDC Error Code: 1015 LED: N/A Description: The Communication Lost Fault bit is set if the fiber-optic communication between the PMI Processor and the UDC module is lost due to two consecutive errors of any type. This bit is set only after communication between the PMI Processor and the UDC module has been established. This bit should be used in the run permissive logic for the drive. Also refer to the CCLK Synchronized bit (register 200/1200, bit 14). 203/1203 Drive Warning Register The warnings indicated by this register cause no action by themselves. Any resulting action is determined by the application task. The user must ensure that the AutoMax application task monitors register 203/1203 and takes appropriate action if any of these conditions occurs. When a werning condition is detected, these bits are latched until the Warning Reset bit (bit 9) of the Drive Control register (register 100/1100) is set. BIt: 0 Hex Value: 0001H Sug. Var. Name: WRN OV@ Range: N/A Access: Read only UDC Error code: N/A LED: N/A Description: The D-C Bus Over Voltage Warning bit is set if the D-C bus voltage rises above the over voltage threshold value stored in local tunable OVT_E0%. The torque is automatically limited to avoid an over voltage fault. Bit 4 of the Drive Warning register will also be set to indicate the torque is being limited by the system. Refer to the appropriate SA3000 Power Modules manual for more information about internal D-C bus control.

203/1203 Drive Warning Register (Continued) Bit 1 Hex Value: 0002H Sug. Var. Name: WRN UV@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The D-C Bus Under Voltage Warning bit is set if the D-C bus voltage drops below the under voltage threshold value stored in local tunable UVT_E0%. The torque is automatically limited to avoid further drop in D-C bus voltage. Bit 4 of the Drive Waming register is also set to indicate the torque is being limited by the system. Refer to the appropriate \$A3000 Power Modules manual for more information about internal D-C bus control. Bit: 2 Hex Value: 0004H Sug. Var. Name: WRN GND@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Ground Current Warning bit is set if ground current exceeds the ground fault current level value stored in local tunable GIT_E1%. Bit: 3 Hex Value: 0008H Sug. Var. Name: WRN VR@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Voltage Ripple Warning bit is set if the ripple on the D-C bus exceeds the voltage ripple threshold value stored in local tunable VRT_E0%. This is intended to be used to detect an input phase loss in the convertor section if three-phase A-C input is used, but can also be used for a common bus supply. Bit: 4 Hex Value: 0010H Sug. Var. Name: WRN_RIL@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: When the drive is in Run Mode, the Reference In Limit Warning bit is set if the reference to the regulator exceeds the maximum value permitted (+/-4095) or is being limited by the system in response to an over voltage or under voltage warning. In Test Mode, this bit is used by the bridge test to indicate an illegal test code. See register 100/1100, bit 2 for additional information on the bridge test. Bit: 5 Hex Value: 0020H Sug. Var. Name: WRN TUN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Tuning Aborted Warning bit is set if any of the automatic tuning procedures (e.g., resolver balance and gain calibration) are not successful.

203/1203 Drive Warning Register (Continued) **Bil:** 6 Hex Value: 0040H Sug. Var. Name: WRN SHR@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Load Sharing Warning bit is set if a problem occurs with current sharing between parallel Power Modules. Bits 13, 14, or 15 in registers 204/1204, 220/1220, or 221/1221 will be set to indicate the phase and the Power Module affected. Bit: 7 Hex Value: 0090H Sug. Var. Name: WRN OT@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Over Temperature Warning bit is set if the warning level thermal switch in the Power Module opens. If Power Modules are connected in parallel, bit 12 is set in register 204/1204, 220/1220, or 221/1221 to indicate which Power Module is affected. Bh: 8 Hex Value: 0100H Sug. Var. Name: WRN_BGD@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Bad Gain Data Warning bit is set if any of the following conditions occur: A current minor loop gain variable or a vector algorithm variable has been modified by the user outside of acceptable limits. The invalid value will be ignored by the system and the last acceptable value entered will be used. For a description of these variables, refer to Appendix B Drive parameter(s) have been loaded that are outside of acceptable limits. This is also part of an interlock test that will prevent the drive from entering the run mode. See register 205/1205, bit 0. The following relationship between the power loss fault threshold (PLT_E0%), the over voltage. warning threshold (OVT_E0%) and the under voltage warning threshold (UVT_E0%) is not true: PLT_E0% < UVT_E0% < OVT_E0%. 4) OVT_E0% > 900V for Medium Power A-C Power Modules or 925V for High Power A-C Power Modules. Bit: 10 Hex Value: 0400H Sug. Var. Name: WRN VOA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Vector Orientation Alignment Warning bit is set if the phase error between PMI A and PMI B is greater than 5 degrees after vector orientation alignment (commanded by register 1100, bit 6) is complete. This bit is used only when SA3000 Parallel Inverters is selected during UDC module configuration. Blt: 12 Hex Value: 1000H Sug. Var. Name: WRN FAN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The PMI Fan Loss Warning bit is set if airflow through the PMI rack is not sensed.

203/1203 Drive Warning Register (Continued) Bit: 13 Hex Value: 2000H Sug. Var. Name: WRN RAL@ Range: N/A Access: Read only UDC Error Code: N/A LED: RAIL FLT on the PMI Processor Description: The Bail Communication Warning bit is set if a rail communication problem occurs and is logged in registers 4, 10, 16, or 22. Refer to tables 3.4 - 3.6. Bit: 14 Hex Value: 4000H Sug. Var. Name: WRN CLK@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The CCLK Not Synchronized Warning bit is set if the CCLK counters in the PMI Processor and the UDC module are momentarily not synchronized. Bit: 15 Hex Value: 8000H Sug. Var. Name: WRN COM@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The PMI Communication Warning bit is set if a fiber-optic communication error between the PMI Processor module and the UDC module occurs. Communication errors in two consecutive messages will cause a drive fault. 204/1204 Power Device Status Register The bits in the Power Device Status register indicate the status of Power Module A and its related hardware. Bits 0 through 5 appty to both Medium Power A-C Power Modules and High Power A C Power Modules, Bits 7 through 15 apply to High Power A-C Power Modules only. When High Power A-C Power Modules are connected in parallel, registers 220/1220 and 221/1221 are used to indicate the status of Power Module Baud Power Module C, respectively. If an overcurrent (IOC) fault occurs, the associated phase status bits are set. If a shoot through fault occurs, the associated phase status bits and the Intelligent Power Module A bit (bit 6) are set. Bit: 0 Hex Value: 0001H Sug. Var. Name: U UPA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U-Upper IOC A bit is set if an overcurrent or shoot through fault occurs in the phase U, upper power devices. Bit: 1 Hex Value: 0002H

Hex Value: 0002H Sug. Var. Name: V_UPA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V-Upper IOC A bit is set if an overcurrent or shoot through fault occurs in the phase V, upper power devices.

204/1204 Power Device Status (Continued) Bit 2 Hex Value: 0004H Sug. Var. Name: W UPA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W-Upper IOC A bit is set if an overcurrent or shoot through fault occurs in the phase W, upper power device, Bit: 3 Hex Value: 0008H Sug. Var. Name: U LOA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U-Lower IOC A bit is set if an overcurrent or shoot through fault occurs in the phase U, lower power device. Bit: 4 Hex Value: 0010H Sug. Var. Name: V LOA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V-Lower IOC A bit is set if an overcurrent or shoot through reult occurs in the phase V. lower power device. Bit: 5 Hex Value: 0020H Sug. Var. Name: W LOA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W-Lower IOC A bit is set if an overcurrent or shoot through fault occurs in the phase W, lower power device. BIC 6 Hex Value: 0040H Sug. Var. Name: IPMA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Intelligent Power Module A bit is set to indicate that a shoo: through fault has occurred in Power Module A. Bits 0-5 of register 204/1204 identity the power device in which the fault occurred. Bit: 7 Hex Value: 0080H Sug. Var. Name: GDIA@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The GDI Fault A bit is set if a problem with the Gate Driver Interface module's power supply occurs. This bit is used with High Power A-C Power Modules only.

204/1204 Power Device Status (Continued)
Bit: 8 Her Value: 0100H
Sug. Var. Name: CHGA:@
Range: N/A
Access: Read only
UDC Error Code: N/A
LED: N/A Departation: The Charge Foull & billio and it a charge has time out foult ecours in Down Medule &
(see register 202/1202, bit 6). This bit is used with High Power A-C Power Modules only.
Bit: 12
Hex Value: 1000H
Sug. Var. Name: OTA@
Range: N/A
Access: Head only
I ED: N/A
Description: The Over Temperature A bit is set if an over temperature fault or warning occurs in Power Module A. This bit is used with High Power A-C Power Modules only.
Bit: 13
Hex Value: 2000H
Sug. Var. Name: U_SHRA@
Range: N/A
Access: Read only
LED: N/A
Description: The Phase U Current Sharing A bit is set if a problem with current sharing occurs on phase U between Power Modules; i.e., Power Module A is not carrying its share of the phase U current. This bit is used with High Power A-C Power Modules only.
Bit: 14
Hex Value: 4000H
Sug. Var. Name: V_SHRA@
Range: N/A
Access: Read only
LED: N/A
Description: The Phase V Current Sharing A bit is set if a problem with current sharing occurs on
phase V between Power Modules: i.e., Power Module A is not carrying its share of the phase V
current. This bit is used with High Power A-C Power Modules only.
Bit: 15
Hex Value: 8000H
Sug. Var. Name: W_SHRA@
Range: N/A
Access: Head only
LED: N/A
Rescription: The Phase W Current Sharing A bit is set if a problem with current sharing occurs on
phase W between Power Modules: i.e., Power Module A is not carrying its share of the phase W current. This bit is used with High Power A-C Power Modules only.

205/1205 Interlock Register Interlock tests are executed whenever bits 0, 1, 2, or 4 of register 100/1100 are set. The first problem detected will be indicated by the corresponding bit in this register. Note that these bits will prevent the torque minor loop from running. Refer to the SA3000 Diagnostics. Troubleshooting, and Start-up Guidelines instruction manual for more information about interlock tests. Bit: 0 Hex Value: 0001H Sug. Var. Name: IC CNF@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Configuration Parameters Not Loaded bit is set if the configuration parameters have not been downloaded into the UDC module from the Programming Executive or the parameters are outside of acceptable limits. Bit: 1 Hex Value: 0002H Sug. Var. Name: IC GAIN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Gains Not Loaded bit is set if the following pre-defined local tunables are zero or a UDC task containing these variables has not been loaded to the rack: SLIP_ADJ_E3%, FLUX WCO%, OVT E0%, UVT E0%, PLT E0%, GIT E1%, IST E1%, STATOR T E4%, STATOR R E4%, STATOR IZ E1%, and CML WOO%. Bit: 2 Hex Value: 0804H Sug. Var. Name: IC RPI@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The RPI Missing bit is set if the Run Permissive Input on the Resolver & Drive I/O module is not on. Bit: 3 Hex Value: 0008H Sug. Var. Name: IC FLT@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Faults Need Reset bit is set if previous faults (register 202/1202) have not been cleared. Bit: 4 Hex Value: 0010H Sug. Var. Name: IC RISE@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Rising Edge Required bit is set if a rising edge is not detected on a command bit in register 100/1100. For example, this bit will be set if the application task has set the Fault Reset bit (register 100/1100, bit 8) but has not cleared and then re-enabled any command bits.

205/1205 Interlock Register (Continued) Bit: 5 Hex Value: 0020H Sug. Var. Name: IC MORE@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The More Than One Request bit is set if more than one operating mode is requested at a time in register 100/1100 (bits 0, 1, 2). Bit: 6 Hex Value: 0040H Sug. Var. Name: IC BUS@ or IC SYN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: If SA3000 Vector or SA3000 Vector with Constant Power is selected during UDC module configuration, bit 6 is used as the Bus Not Ready bit (IC_BUS@). The Bus Not Ready bit is set when turning on the drive if the D-C bus is not ready. The bus is ready when the D-C bus voltage is greater than the under voltage threshold value stored in local tunable UVT_E0% and has reached a steady state, and feedback indicates that the pre-charge contactor has closed. This bit will also be set when turning on the drive if the bus enable bit (register 100/1100, bit 4) has not been set. Refer to the appropriate SA3000 Power Modules manual for more information about internal D-C bus control. If SA3000 Parallel Inverters is selected during UDC module configuration, bit 6 is used as the Sync. Not Ready bit. The Sync Not Ready bit is set if the torgue loop is enabled and PMI B's vector orientation has not been aligned with that of PMI A. Refer to the Vector Orientation Alignment. Request bit (register 100/1100, bit 6) for more information. Bit: 7 Hex Value: 0060H Sug. Var. Name: IC MCR@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The MCR Did Not Close bit is set if the output contactor did not close when commanded to. (Note that the output contactor is optional.) Bit: 8 Hex Value: 0100H Sug. Var. Name: IC GDI@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The GDI Mismatch bit is set if, when turning on the drive, the number of Gate Driver Interface (GDI) modules in the rack does not match the number configured or the GDI modules have been placed incorrectly in the rack. Refer to the PMI Rack instruction manual for the correct module placement. The GDI Mismatch bit is set if, when turning on the bridge test, a Power Module has not been selected for the test (bit 10, 11, or 12 in register 100/1100) or the incorrect Power Module has been selected (e.g., Power Module C has been selected, but the drive contains only two Power Modules connected in parallel). Bit: 9 Hex Value: 0200H Sug. Var. Name: IC IPBP@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The incompatible PMI Backplane bit is set if the PMI rack contains an incorrect backplane (e.g., B/M O 60003).

205/1205 Interlock Register (Continued) Bit: 10 Hex Value: 0400H Sug. Var. Name: IC_IRES@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Incompatible Resolver bit is set if the PMI Rack contains Resolver & Drive I/O modules B/M 60001 or B/M 60001-1.

206/1206 D-C Bus Voltage (Volts) Register

Hex Value: N/A Sug. Var. Name: BUS_VDC% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The D-C Bus Voltage (Volts) register displays the voltage of the D-C bus in volts.

207/1207 D-C Bus Current (Amps) Register

Hex Value: N/A Sug. Var. Name: BUS_IDC% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The D-C Bus Current (Amps) register displays the measured current in the D-C bus. The displayed value is equal to the number of amps times 10. For example, 50.1 amps would be displayed as 501.

208/1208 Ground Current Feedback (Amps) Register

Hex Value: N/A Sug. Var. Name: GI_FB% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Ground Current Feedback (Amps) register displays the measured RMS ground current. The displayed value is equal to the number of amps times 10. For example, 50.1 amps would be displayed as 501.

209/1209 Voltage Feedback (Volts RMS) Register

Hex Value: N/A Sug. Var. Name: V_FB% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Voltage Feedback (Volts RMS) register displays the measured RMS motor voltage in volts.

210/1210 Current Feedback (Amps RMS) Register

Hex Value: N/A Sug. Var. Name: I_FB% Range: N/A Access: Read only UDC Error Code: N/A

LED: N/A

Description: The Current Faedback (Amps RMS) register displays the measured RMS motor current feedback. The displayed value is equal to the number of amps times 10. For example, 50.1 amps would be displayed as 501.

211/1211 Current Feedback (Normalized) Register

Hex Value: N/A Sug. Var. Name: I_FBN% Range: +/-4095 Access: Read only UDC Error Code: N/A LED: N/A

Description: The Current Feedback (Normalized) register displays the measured RMS motor current. This data is normalized so that +/- 4095 counts is equal to the maximum RMS motor current as calculated in Appendix E. This register is used as the LEDBK parameter in the THERMAL OVERLOAD control block used in DPS drives to monitor the motor for thermal overfoad.

212/1212 Id Feedback (Normalized) Register

Hex Value: N/A Sug. Var. Name: ID_FBN% Range: 4095 Access: Read only UDC Error Code: N/A LED: N/A Description: The Id Feedback (Normalized) register displays the Id component (magnetizing current) of the current feedback. This data is normalized so that 4095 counts is equal to the full value of magnetizing current (STATOR_IZ_E1%).

213/1213 Iq Feedback (Normalized) Register

Hex Value: N/A Sug. Var. Name: IQ_FBN% Range: +/-4095 Access: Read only UDC Error Code: N/A LED: N/A Description: The Iq Feedback (Normalized) register displays the Iq (torque-producing) component of the current feedback. This data is normalized so that +/-4095 counts corresponds to lorque reference (TRO_REF%).

214/1214 User Analog Input Register

Hex Value: N/A Sug. Var. Name: ANA_IN% Renge: -2047 (-10V) to -2047 (+10V) Access: Read only UDC Error Code: N/A LED: N/A Description: The User Analog Input register displays the measured user analog input value from the Resolver Feedback connector on the Resolver & Drive I/O module.

215/1215 Resolver Scan Position Register

Hex Value: N/A Sug. Var. Name: RES_SCN_POS% Range: -32768 to 32767 corresponding to the resolver's position Access: Read only UDC Error Code: N/A LED: N/A Description: The Resolver Scan Position register displays the electrical position of the resolver at the beginning of the UDC task scan. This register is reset to zero at power up.

216/1216 Resolver Strobe Position Register

Hex Value: N/A Sug. Var. Name: RES_STR_POS% Range: -32768 to 32767 corresponding to the resolver's position Access: Read only UDC Error Code: N/A LED: N/A Description: The Resolver Strobe Position register displays the electrical position of the resolver at the time a strobe signal is detected.

217/1217 Revolutions Per Minute Register or Id Feedback Register

Hex Value: N/A Sug. Var. Name: RPM% or ID_FBK% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A

Description: If SA3000 Vector or SA3000 Vector with Constant Power is selected during the UDC module configuration, register 217/1217 is used as the Revolutions Per Minute register (RPM%). The Revolutions Per Minute register displays the speed of the motor in RPM. It is not intended for closed loop control. A positive number in this register indicates a forward direction; a negative number indicates the reverse direction.

If SA3000 Parallel Inverters is selected during UDC module configuration, register 217 is used as the Id Feedback register. The Id Feedback register contains the Id reference value calculated by PMLA and is displayed as peak amps E1. This value is copied into register 1104 by the drive B UDC task so that it is also used as PMI B's Id reference. Refer to section 4.2.4 and Appendix C for more information on SA3000 Parallel Inverters.

Note that motor RPM data is available through register 219/1219 by selecting that variable for output on meter port 4.

218/1218 Slip Feedback Register or Vector Orientation Feedback Register

Hex Value: N/A Sug. Var. Name: SLIP_FB% or VO_FBK% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: If SA3000 Vector or SA3000 Ve

Description: If SA3000 Vector or SA3000 Vector with Constant Power is selected during UDC module configuration, register 218/1218 is used as the Slip Feedback register (SLIP_F8%). The Skp Feedback register displays the amount of rotor slip. The displayed value is equal to hertz times 100. For example, SHz would be displayed as 500.

If SA3000 Parallel Inverters is selected during UDC module configuration, register 218 is used as the Vector Orientation Feedback register. The Vector Orientation Feedback register contains PMI A's commanded phase angle where 1023 = 2*n*. This value is copied into register 1107 by the drive B UDC task for comparison to PMI B's phase angle. Refer to section 4.2.4 and Appendix C for more information on SA3000 Parallel Inverters.

Note that slip frequency data is available through register 219/1219 by selecting that variable for output on meter port 4.

219/1219 Selected Variable Register Hex Value: N/A Sug. Var. Name: SEL VAR% Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: This register displays the value of the actual variable that is selected for display on PMI meter port four. This allows monitoring of data in the UDC module that is normality only available in the PMI rack. Refer to chapter 2 for more information on displaying variables on the PMI Processor's meter ports. 220/1220 Parallel Power Module B Status Register The bits in the Parallel Power Module B Status register indicate the status of Power Module B and its related hardware. This register is used only when High Power A-C Power Modules are connected in parallel. If an overcurrent (IOC) fault occurs, the associated phase status bits are set, if a shoot through fault occurs, the associated phase status bits and the Intelligent Power Module 8 bit (bit 6) are sat. Bit: 0 Hex Value: 0001H Sug. Var. Name: U UPB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U-Upper IOC B bit is set if an overcurrent or shoot through fault occurs in the phase U, upper power device. Bit 1 Hex Value: 0002H Sug. Var. Name: V UPB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V-Upper IOC B bill is set if an overcurrent or shoot through fault occurs in the phase V. upper power device. Bit 2 Hex Value: 0004H Sug. Var. Name: W UPB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W-Upper IOC B bit is set if an overcurrent or shoot through fault occurs in the phase W, upper power device. Bit: 3 Hex Value: 0008H Sug. Var. Name: U LOB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U-Lower IOC B bit is set if an overcurrent or shoot through fault occurs in the phase U. lower power device.

220/1220 Parallel Power Module B Status Register (Continued) Bit: 4 Hex Value: 0010H Sug. Var. Name: V LOB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V Lower IOC B bit is set if an overcurrent or shoot through fault occurs in the phase V, lower power device. Bit: 5 Hex Value: 0020H Sug. Var. Name: W LOB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W-Lower IOC 8 bit is set if an overcurren: or shoot through fault occurs in the phase W, lower power device. Bit: 6 Hex Value: 0040H Sug. Var. Name: IPMB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Intelligent Power Module B bit is set to indicate that a shoot through fault has occurred in Power Module B. Bits 0-5 of register 220/1220 identify the power device in which the fault occurred. Bit: 7 Hex Value: 0080H Sug. Var. Name: GDIB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The GDI Fault B bit is set if a problem with the Gate Driver Interface module's power supply occurs. Bit 6 Hex Value: 0100H Sug. Var. Name: CHGB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Charge Fault 8 bit is set if a charge bus time-out fault occurs in Power Module B (see register 202/1202, bit 6).

220/1220 Parallel Power Module B Status Register (Continued) Bit: 12 Hex Value: 1000H Sug. Var. Name: OTB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Over Temperature B bit is set if an over temperature fault or warning occurs in Power Module B. Bit: 13 Hex Value: 2000H Sug. Var. Name: U SHRB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U Current Sharing B bit is set if a problem with current sharing occurs on phase U between Power Modules; i.e., Power Module B is not carrying its share of the phase U current. Bit 14 Hex Value: 4000H Sug. Var. Name: V SHRB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V Current Sharing B bit is set if a problem with current sharing occurs on phase V between Power Modules; i.e., Power Module B is not carrying its share of the phase V current. Bit: 15 Hex Value: 8000H Sug. Var. Name: W SHRB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W Current Sharing B bit is set if a problem with current sharing occurs on phase W between Power Modules; i.e., Power Module B is not carrying its share of the phase W current. 221/1221 Parallel Power Module C Status Register

The bits in the Parallel Power Module C Status register indicate the status of Power Module C and its related hardware. This register is used only when High Power A-C Power Modules are connected in parallet.

If an overcurrent (IOC) fault occurs, the associated phase status bits are set. If a shoot through fault occurs, the associated phase status bits and the Intelligent Power Module C bit (bit 6) are set.

Bit: 0 Hex Value: 0001H Sug. Var. Name: U_UPC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U-Upper IOC C bit is set if an overcurrent or shoot through fault occurs in the phase U, upper power device.

221/1221 Parallel Power Module C Status Register (Continued) Bit: 1 Hex Value: 0002H Sug. Var. Name: V UPC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V-Upper IOC C bit is set if an overcurrent or shoot through fault occurs in the phase V, upper power device. Bit: 2 Hex Value: 0004H Sug. Var. Name: W UPC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W-Upper IOC C bit is set if an overcurrent or shoot through fault occurs in the phase W, upper power device. Bit: 3 Hex Value: 0008H Sug. Var. Name: U LOC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U-Lower IOC C bit is set if an overcurrent or shoot through fault occurs in the phase U, lower power device. 65 Bit: 4 Hex Value: 0010H Sug. Var. Name: V LOC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V-Lower IOC C bit is set if an overcurrent or shoot through fault occurs in the phase V, lower power device. Bit: 5 Hex Value: 0020H Sug. Var. Name: W LOC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W-Lower IOC C bit is set if an overcurrent or shoet through fault occurs in the phase W, lower power device.

221/1221 Parallel Power Module C Status Register (Continued) Bit: 6 Hex Value: 0040H Sug. Var. Name: IPMC@ Range: N/A Access: Reed only UDC Error Code: N/A LED: N/A Description: The Intelligent Power Module C bit is set to indicate that a shoot through fault has occurred in Power Module C. Bits 0-5 of register 221/1221 Identify the power device in which the fault occurred. Bit: 7 Hex Value: 0080H Sug. Var. Name: GDIC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The GDI Fault C bit is set if a problem with the Gate Driver Interface module power supply occurs. BIt: B Hex Value: 0100H Sug. Var. Name: CHGC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Charge Fault C bit is set if a charge bus time-ou: fault occurs in Power Module C (see register 202/1202, bit 6). Bit: 12 Hex Value: 1000H Sug. Var. Name: OTC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Over Temperature C bit is set if an over temperature warning or fault occurs in Power Module C. Blt: 13 Hex Value: 2000H Sug. Var. Name: U SHRC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase U Current Sharing C bit is set if a problem with current sharing occurs on phase U between Power Modules; i.e., Power Module C is not carrying its share of the phase U current. Bit: 14 Hex Value: 4000H Sug. Var. Name: V SHRC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase V Current Sharing C bit is set if a problem with current sharing occurs on phase V between Power Modules; i.e., Power Module C is not carrying its share of the phase V current.

221/1221 Parallel Power Module C Status Register (Continued) Bit: 15 Hex Value: 8000H Sug. Var. Name: W_SHRC@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Phase W Current Sharing C bit is set if a problem with current sharing occurs on phase W between Power Modules; i.e., Power Module C is not carrying its share of the phase W current.

3.5 Application Registers (Registers 300-599, Every Scan) (Registers 1300-1599, Every Nth Scan)

The application registers are used to pass application-specific data between an AutoMax Processor and the UDC module.

Memory is allocated for a maximum of 600 application registers which are used by both tasks (A and B). There are 300 registers that can be used every scan (registers 300-599) and 300 registers that can be used every Nth scan (registers 1300-1599). "N" is defined in register 2001. Note that the status of application registers is not relained after a Stop All.

Application registers 300-599 can be used every scan of UDC tasks. Registers within this range written to by a UDC task are updated by the UDC operating system from its local memory to cual port memory after each task is run. Registers within this range written to by an AutoMax task are read by the UDC operating system from duel port memory and copied into the UDC local memory at the beginning of each scan in order to have a consistent context for evaluation. See figure 3.1.

WARNING

IF YOU USE DOUBLE INTEGER VARIABLES, YOU MUST IMPLEMENT A SOFTWARE HANDSHAKE BETWEEN THE TRANSMITTER AND THE RECEIVER TO ENSURE THAT BOTH THE LEAST SIGNIFICANT AND MOST SIGNIFICANT 16 BITS HAVE BEEN TRANSMITTED BEFORE THEY ARE READ BY THE RECEIVING APPLICATION PROGRAM. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN BODILY INJURY OR DAMAGE TO EQUIPMENT.



Figure 3.1 - Typical UDC Task Scan

Note that the same bits or registers must not be written to (and used as outputs) by both an AutoMax task and a UDC task.

Application registers 1300-1599 can be used every Nth scan of the UDC task. Nth scan registers should be used when it is necessary to synchronize one or more UDC tasks to an AutoMax task.

The registers within this range (1300-1599) that are written to by a UDC task are updated by the UDC operating system from its local memory to dual port memory at the end of the scan that occurs before the Nth scan (N-1). At that time, an interrupt will be generated by the UDC operating system to indicate that new data has been written to the dual port memory. Refer to the 2000-series registers for more information on interrupts. An AutoMax task must have defined a hardware EVENT in order to be able to respond to an interrupt from the UDC module. Registers within this range that are written to by an AutoMax task are read by the UDC operating system from dual port memory and copied into the UDC local memory at the beginning of the Nth scan. See figure 3.2.


Figure 3.2 - Nth Scan Interrupts

The following data types can be defined in the application register area: boolean (bit), integer (16 bits), double integer (32 bits), and real (32 bits). Because of the way in which read and write operations occur in the UDC dual port memory, however, the programmer must assign boolean variables carefully within pairs of 16-bit registers.

The UDC operating system generally operates on the amount of memory called for by the data type. e.g., when it is requested to write to a 16-bit (integer) value, it writes only to those specific 16 bits. However, in the case of boolean variables, the UDC operating system always operates on 32 bits at a time. It is not possible for the operating system to write to only one bit within a register. The remaining 31 bits in the register pair will be written over as well, possibly resulting in corrupted data.

Within any pair of 16-bit registers beginning on an even number boundary, i.e., registers 300 and 301, 302 and 303 (but not registers 301 and 302), all boolean variables must be either inputs or outputs. If there are no bits assigned within a particular register pair, then one 16-bit register can be an output and the other 16-bit register can be an input, or both can be inputs or outputs. Alternatively, the entire register pair can be delined as a real or double integer value.

Note that if you are referencing a 32-bit value (real or double integer) in the UDC dual port from an AutoMax task, the operation is being performed by the AutoMax Processor, which operates on 16 bits of data at a time. In such a situation, you must employ some form of software handshaking in the AutoMax task to ensure that both the upper and lower order 16 bits represent the current value of the variable. This is required for 32-bit values in the "every" scan register range. It is possible to use software "flags" to indicate that data can be read. It is also possible to read the data multiple times (typically three times) and compare the values.

3.6 UDC Module Test I/O Registers (Registers 1000-1017)

This view is used to configure the UDC module's Test Switch Inputs Register and the Meter Port Setup Registers.

3.6.1 UDC Module Test Switch Inputs Register (Register 1000)

This view is used to configure the register that displays the status of the test switches and LED indicators on the UDC module. Writing to this register will not change the state of the UEDs. The status of this register is retained during a Stop Ail.

Bil: D Hex Value: 0001H Sug. Var. Name: UDC PB@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Pushbutton Input bit is on when the pushbutton is pressed. Bit 1 Hex Value: 0002H Sug, Var. Name: SWIT UP@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Switch Up Input bit is on when the switch is in the up position.

1000 UDC Test Switch Inputs Register (Continued) Bit: 2 Hex Value: 0004H Sug. Var. Name: SWIT DN@ Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Switch Down Input bit is on when the switch is in the down position. Bit: 8 Hex Value: 0100H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: OS OK on the UDC module Description: Status of the Operating System OK LED on the UDC module (0 - Off; 1 - On). Bit 9 Hex Value: 0200H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: COMM A OK on the UDC module Description: Status of the COMM A OK LED on the UDC module (0 = Off; 1 = On). Bit: 10 Hex Value: 0400H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: DRV A FLT on the UDC module **Description:** Status of the Drive A Fault LED on the UDC module (0 = Off; 1 = On). Bit: 11 Hex Value: 0800H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: COMM B OK on the UDC module Description: Status of the COMM B OK LED on the UDC module (0 = Off; 1 = On). Bit: 12 Hex Value: 1000H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: DRV B FLT on the UDC module **Description:** Status of the Drive B Fault LED on the UDC module (0 = Off; 1 = On).

3.6.2 UDC Module Meter Port Setup Registers (Registers 1001-1017)

Registers 1001-1017 are used to configure the UDC module's meter ports. This configuration determines what variables from the UDC module's dual port memory are to be displayed on the meter ports at the end of the UDC scan. At system power-up, the output values of the ports are reset to zero.

To map a UDC variable to a specific meter port at power-up, refer to table 3.7 and use the following procedure. Note that the setup register configurations are retained during a Stop All.

UDC Module Meter Port Setup Registers	Meter Port 1	Meter Port 2	Meter Port 3	Meter Port 4
Variable Register Number Register	1002	1006	1010	1014
Bit Number Register	1003	1007	1011	1015
Maximum Value Register	1004	1008	1012	1016
Minimum Value Register	1005	1009	1013	1017
Change Setup Register	1001	1001	1001	1001

Table 3.7 - UDC Module	Meter Port	Setup	Registers
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For each meter port:

- Step 1. Place the register number of the variable you wish to display in the appropriate Variable Register Number register.
- Step 2. If an individual bit of the register is to be displayed, enter it in the Bit Number register as 100 (bit 00) to 115 (bit 15).

If the entire register is to be displayed, enter a value of zero in the Bit Number register.

- Step 3. Place the value (maximum 32767) that will represent +10V in the Maximum Value register.
- Step 4. Place the value (minimum 32767) that will represent 10V in the Minimum Value register.
- Step 5. Set register 1001 (Initiate Change in Setup) equal to a non-zero value to store the new setup register configurations in memory.

The UDC module's meter ports are updated once per scan once the UDC task is running and CCLK is on. They are updated every 5 milliseconds when CCLK is off.

UDC meter ports can also be set up on-line using the "Satup UDC" selection from the Monitor monu as described in the AutoMax Programming Executive instruction manual. This setup is valid only until there is a power cycle, in which case the meter ports default to outputting zero voltage and the UDC Setup screen is cleared on power-up.

Refer to the UDC Module instruction manual (S-3007) for more information about the UDC module's meter ports.

3.6.2.1 Resolution of Meter Port Data

For meter ports, the output values will be clamped at the outside (+/- 10V) limits. Note that if you select to display a data range that is narrower than the actual range of the data, your output values will not change until the value returns to within the range you selected to display. In other words, data is being updated at the rate described above, but the actual output voltage may not change.

If the actual data being sent to the meter port is significantly smaller than the upper and lower limits assigned by the programmer, the effective resolution of the 8-bit D/A circuit (1 part in 255) will degrade. To calculate the step change indicated on the meter port, calculate the sum of the absolute values of the upper and lower limits (the entire range of possible values) assigned to the port. Then scale this number by 255 in order to determine the minimum step change that will cause the D/A output to change. For example, suppose the programmer sets the +10V and -10V limits at +4095 and -4095, respectively, but the actual value varies only between + 1024 and > 1024. Then:

8190/255 = 32 counts

This means that although the actual data is being updated, the meter port output will change only when the data changes by 32 or more counts. This level of granularity might be acceptable if the range of the data were actually 8190 counts, but might not be acceptable if the data range is only 4095 counts. If the programmer had assigned the limits $\pm/-1024$, the D/A output step change would be only 8 counts: 2048/255 = 8.

1001 Initiate Change in Setup Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register equal to a non-zero value to store the new setup register configurations in UDC memory. You must use this register whather you are changing the meter port setup via an application task or via I/O Monitor.

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1002	UDC Module Meter Port 1 Register Number Register
Hex Valu	e: N/A
Sug. Var.	Name: N/A
Range: N	I/A
Access:	Read/Write
UDC Err	ar Code: N/A
LED: N/A	
Descript	ion: UDC register number (0-2044) to be mapped to mater port 1.
1003	UDC Module Meter Port 1 Bit Number Register
Hex Valu	e: N/A
Sug. Var.	Name: N/A
Range: N	I/A
Access:	Read/Write
UDC Erro	or Code: N/A
LED: N/A	
Descripti	on: Bit number of the UDC register specified in register 1002 that is to be mapped to port 1.
Enter a va	alue of 100 (bit 00) to 115 (bit 15) as required. Enter a value of zero if all of the register's bits
are to be	displayed.
1004	UDC Module Meter Port 1 Meximum Value Register
Hex Valu	e: N/A
Sug. Var.	Name: N/A
Range: h	I/A
Access:	Read/Write
UDC Erro	or Code: N/A
LED: N/A	
Descript is 32767.	ion: Set this register to the number that will represent - 10V. The maximum allowable value
1005	UDC Module Meter Port 1 Minimum Value Register
Hex Valu	e: N/A
Sug. Var.	Name: N/A
Hange: N	I/A
	ReadWrite
Access:	
Access: UDC Erro	7 Code: N/A
Access: UDC Erro LED: N/A	or Code: N/A

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1006 UDC Module Meter Port 2 Register Number Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: UDC register number (0-2044) to be mapped to meter port 2.

1007 UDC Module Meter Port 2 Bit Number Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Bit number of the UDC register specified in register 1006 that is to be mapped to port 2. Enter a value of 100 (bit 00) to 115 (bit 15) as required. Enter a value of zero if all of the register's bits are to be displayed.

1008 UDC Module Meter Port 2 Maximum Value Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register to the number that will represent +10V. The maximum allowable value is 32767.

1009 UDC Module Meter Port 2 Minimum Value Register

2

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register to the number that will represent =10V. The minimum allowable value is =32768.

1010 UDC Module Meter Port 3 Register Number Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: UDC register number (0-2044) to be mapped to meter port 3.

1011 UDC Module Meter Port 3 Blt Number Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Bit number of the UDC register specified in register 1010 that is to be mapped to port 3. Enter a value of 100 (bit 00) to 115 (bit 15) as required. Enter a value of zero if all of the register's bits are to be displayed.

1012 UDC Module Meter Port 3 Maximum Value Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register to the number that will represent – 10V. The maximum allowable value is 32767.

1013 UDC Module Meter Port 3 Minimum Value Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register to the number that will represent -10V. The minimum allowable value is -32768.

1014 UDC Module Meter Port 4 Register Number Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: UDC register number (0-2044) to be mapped to meter port 4.

1015 UDC Module Meter Port 4 Bit Number Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Bit number of the UDC register specified in register 1014 that is to be mapped to port 4. Enter a value of 100 (bit 00) to 115 (bit 15) as required. Enter a value of zero if all of the register's bits are to be displayed.

1016 UDC Module Meter Port 4 Maximum Value Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register to the number that will represent +10V. The maximum allowable value is 32767.

1017 UDC Module Meter Port 4 Minimum Value Register

Hex Value: N/A Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Set this register to the number that will represent -10V. The minimum allowable value is -32768.

3.7 Interrupt Status and Control Registers (Registers 2000-2047)

This view is used to configure registers that control the operation of interrupts to a task on an AutoMax Processor in the rack and to enable CCLK in the rack. These registers are used for Drive A and B. Only one UDC task should write to these registers. Note that the status of these registers is not retained after a Stop All.

2000	Interrupt Status Control Register
Hex Valu Sug. Va Range: Access: UDC En LED: N/ Descrip be writh	ue: N/A r. Name: UDC_ISCR% N/A See individual bits for Code: N/A A tion: The Interrupt Status Control register contains the following information. Only bit 6 can en to by the user . All other bits are read only.
Bit: 0 Hex Vali Sug. Val Range: I Access: UDC En LED: N// Descrip	ue: 0001H r. Name: N/A N/A Read only f or Code: N/A A tion: Interrupt Line Identification.
Bit: 1 Hex Vali Sug. Val Range: Access: UDC Err LED: N// Descrip	ue: 0002H r. Name: N/A N/A Read only ror Code: N/A A tion: Interrupt Line identification.
Bit: 2 Hex Valu Sug. Val Range: Access: UDC En LED: N// Descrip	ue: 0004H r. Name: N/A N/A Read only for Code: N/A A tion: Interrupt Allocated.
Bit: 4 Hex Valu Sug. Val Range: Access: UDC En LED: N// Descrip	ue: 0010H r. Name: N/A N/A Read only ror Code: N/A A tion: Interrupt Generaled This Scan.

2000 Interrupt Status Control Register (Continued) Bit 5 Hex Value: 0020H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: CCLK Counting. Bit 6 Hex Value: 0040H Sug. Var. Name: N/A Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: Enable CCLK on the Multibus Backplane - CCLK must be enabled in the rack for the UDC module to execute its task(s) and communicate synchronously with the PMI. Only one module per rack should enable CCLK. If CCLK is enabled on multiple modules in the rack, an overtap error will result (error code 38). Other modules that can enable CCLK include the M/N 57C409, 57C421, and the 57C411. The UDC module uses CCLK to determine when it should run its tasks. CCLK is also used as the time reference for all UDC modules in the rack so that they are all synchronized to start at deterministic time periods, if interrupts to the AutoMax Processor are required, register 2001 must be set to the desired value before CCLK is enabled. Bit: 7 Hex Value: 00B0H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Interrupt Enabled bit, when set to one by the operating system, indicates that a hardware EVENT has been defined in an AutoMax task. No other programming is required for the UDC operating system to generate an interrupt in the interval defined in register 2001. Bit: 15 Hex Value: 8000H Sug. Var. Name: N/A Range: N/A Access: Read only UDC Error Code: N/A LED: N/A Description: The Interrupt Status bit, when set to one, indicates that an interrupt is being generated at this time. 2001 Scans Per Interrupt Register

Sug. Var. Name: SPI% Range: N/A Access: Read/Write UDC Error Code: N/A LED: N/A Description: The Scans Per Interrupt register comains the number of times a UDC task is to be scanned between updates of the Nth scan application registers. Note that you must write the desired value to this register before you turn on CCLK. The default value is zero (i.e., not applicable because an interrupt is not being used but is updated each scan). One is an allowable value. If a hardware EVENT is defined in an AutoMax application task, this register will also specify when the interrupt occurs, i.e., every Nth scan. See chapter 4 and figure 4.9 for more information on Interrupts. Note that in this register, one scan is a complete scan of both tasks A and B.

Hex Value: N/A

4.0 APPLICATION PROGRAMMING FOR DPS DRIVE CONTROL

DANGER

ONLY QUALIFIED ELECTRICAL PERSONNEL FAMILIAR WITH THE CONSTRUCTION AND OPERATION OF THIS EQUIPMENT AND THE HAZARDS INVOLVED SHOULD INSTALL, ADJUST, OPERATE, OR SERVICE THIS EQUIPMENT. READ AND UNDERSTAND THIS MANUAL AND OTHER APPLICABLE MANUALS IN THEIR ENTIRETY BEFORE PROCEEDING. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN SEVERE BODILY INJURY OR LOSS OF LIFE.

WARNING

ONLY QUALIFIED RELIANCE PERSONNEL OR OTHER TRAINED PERSONNEL WHO UNDERSTAND THE POTENTIAL HAZARDS INVOLVED MAY MAKE MODIFICATIONS TO THE APPLICATION TASKS. ANY MODIFICATIONS MAY RESULT IN UNCONTROLLED MACHINE OPERATION. FAILURE TO OBSERVE THESE PRECAUTIONS COULD RESULT IN DAMAGE TO EQUIPMENT AND BODILY INJURY.

Distributed Power Drive products are sold only as part of engineered systems. The application programming required for each engineered system is developed in response to each customer's specifications. Information in this chapter is general enough to apply to most engineered systems: however, implementation details may vary. Always refer to your wiring diagrams for specific information about your engineered system.

4.1 AutoMax Tasks

AutoMax tasks are used to implement safety interlocks, coordinate multiple UDCs, and collect data from UDC modules in the rack. They can access all common memory and I/O in the AutoMax rack, Including the dual port memory in the UDC module. AutoMax drive control tasks are generally written in PC/Ladder Logic language. Typically, these tasks control the Drive Control register (100/1100) and the I/O Control register (101/1101). AutoMax tasks can access registers in the UDC's dual port memory in the same way as tasks on the UDC module itself, i.e., by declaring them COMMON.

4.2 UDC Tasks

UDC tasks operate on registers in the UDC dual port memory described in chapter 3, as well as on local task-specific variables in order to control some application variable (e.g., speed) and to calculate the required reference values for the selected control algorithm. The UDC task is sometimes referred to as an "outer" or "major" control loop. Note, however, that there may be more than one outer loop per task. In this case the control loops are nested, or "cascaded," within the UDC task.

UDC tasks must be written in the Control Block language, a language designed specifically for drive control. To differentiate them from Control Block tasks written for AutoMax Processors, they must be specified as UDC tasks in the Programming Executive software. Like Control Block tasks on AutoMax Processors, UDC tasks can include a number of BASIC language statements and functions; however, those that allow task suspension or delay are not supported.

UDC tasks are created, compiled, loaded, and monitored in the same way as Control Block tasks for AutoMax Processors. UDC task variables can be monitored, set, tuned, and forced like AutoMax task variables. Note that the UDC module is accessed for monitoring and loading purposes through the serial port on the leftmost AutoMax Processor (or over the DCS-NET network), which is used for all connections to the rack. Any UDC dual port register that is to be used in a UDC task must be defined as COMMON in the task. Recall that UDC dual port memory registers are either reserved for a specific use such as rail data, or available for application-specific purposes to the programmer. Registers that are not specifically identified in one of these two ways in the Programming Executive software or in this instruction manual must not be written to by either the UDC or AutoMax tasks because they are being used by the operating system.

Generally, the common variables on the UDC module are either written to only by AutoMax tasks ("read only" to UDC tasks), or they are written to only by a UDC task ("read only" to AutoMax tasks). The former are typically variables that control an action, e.g., requesting the minor loop to run, and the latter are typically status variables, e.g., indicating the status of the fiber-optic communication link.

UDC tasks can access only the UDC module's own dual port memory. They cannot access other variables in the rack unless an AutoMax task writes those variable values to the application-specific registers in the UDC dual port.



Figure 4.1 illustrates one UDC task scan.

Figure 4.1 - Typical UDC Task Scan

All common input values for task A are first read from the dual port memory and then stored in a local buffer in order to have a consistent context for evaluation. Task A is then executed. After task A has been executed, the common output values from task A are written from the local memory buffer to dual port memory. All common input values for task B are then read from dual port memory and stored in a local buffer in order to have a consistent contaxt for evaluation. Task B is then executed. Note that task B can act on task A outputs within one scan. After task B has been executed, the common output values from the local memory buffer to dual port memory.

The only exception to this pattern are the common variables in the "Nth" scan application register area. These registers are updated immediately before every "Nth" scan only, as delined by the user. See section 4.3 and figure 4.3 for more information on "Nth" scan interrupts. See section 4.2.3 for more information on the command and feedback messages.

4.2.1 Typical Structure of a UDC Task

The typical structure of a UDC task is described below. The first part of the task, described in steps 1 to 4 below, is considered task initialization. This part of the task will only run on the initial scan of the task or on any subsequent re-start.

1. Local and common variable definitions

This section of the task defines names for values internal to the task (LOCALs) and all UDC dual port memory registers used in the task (COMMONs).

2. Pre-delined local lunable variable definitions

This section defines the variables that are used by the PMI for functions such as tuning the control algorithm and calibrating the resolver. The UDC task "skeleton" file in the Programming Executive software includes these local tunable definitions. See section 4.2.2 and Appendix B for more information.

- 3. Initialization
 - a) UDC Meter Port set-up: The registers whose values will be output on the UDC Meter Ports are defined here. These registers can also be defined on-line using the Programming Executive software (optional).
 - b) Scans per update definition: The scans-per-update register (2001 for both drive A and B) is defined to tell the UDC Processor when to update the Nth scan registers, and optionally, also when to interrupt an AutoMax Processor task that has defined a hardware EVENT tied to the UDC's interrupt register. The AutoMax task can then read from and write to the UDC dual port memory registers on a deterministic basis, and coordinate with the other tasks in the system (optional).
 - c) Any other initialization required for the application.

This portion of the task (steps 1-3), before the SCAN_LOOP block, only executes the first time that the task is scanned, after a STOP ALL command and subsequent Run command, or after power is cycled to the rack.

SCAN LOOP block/Enabling CCLK.

This control block tells the UDC operating system how often to execute the task based on the constant clock (CCLK) signal on the rack backplane. Note that the CCLK signal must be enabled by a task in the rack before any UDC tasks in the rack can be scanned beyond their SCAN_LOOP blocks. Note that CCLK must be enabled again after a STOP ALL in the rack. CCLK is enabled by setting the appropriate "CCLK enable" bit on certain modules in the rack, such as the UDC module. CCLK must be enabled on one module only. If CCLK is enabled on multiple modules in the rack, an overlap error will result (error code 38).

The UDC task runs based on "ticks;" one tick is equal to one 500 µsec (.5 msec) CCLK interval. The value can range from 1 to 20 ticks.

The programmer must specify how often the task should run in the TICKS parameter of the SCAN_LOOP block in the task itself. The TICKS value represents the number of 500 used intervals within which the task must execute or an overlap error will occur. In order to calculate this value, both drive A and drive B tasks must be considered together because they execute one Immediately following the other (A, then B). See figure 4.1 for more information.

When determining the value to enter, the programmer must consider how long it will take both tasks to actually run, allow some time for processing overhead, and use the resulting value to determine the TICKS value for the SCAN_LOOP block in both the drive A and drive B tasks. The AutoMax Control Block Language manual (J-3676) lists the execution times of the Control Blocks.

For example, if the programmer assigns UDC task A a TICKS parameter of 8 (4 ms.), then UDC task B must also have TICKS defined at 8, and both tasks must be able to execute within an 8 tick window of time, or an overlap error will result and all tasks in the rack will stop. If the tick rates do not match, error code "956" will be reported for one or both tasks in the error log and all tasks in the rack will be stopped.

Note that, unlike Control Block tasks on AutoMax Processors, UDC tasks cannot run on a hardware or software event basis. The EVENT parameter cannot be specified in the SCAN_LOOP block in UDC tasks. This means that there is no timeout for execution of the UDC tasks. If the UDC task is scanned to the SCAN_LOOP block and CCLK is not on, the task will simply wait without timing out.

Note that no other control blocks are permitted before the SCAN_LOOP block. BASIC statements, however, are permitted before the SCAN_LOOP block.

5. Other Control Block and BASIC statements or functions

This portion of the task consists of the logic specifically required for the application. This portion of the UDC task (after the SCAN_LOOP block) is the only part of the task that executes after the initial scan of the task, after a STOP ALL command and subsequent Run command, or after power is cycled to the rack.

6. Motor thermal overload protection

Electronic thermal overload protection for Distributed Power drives is normally provided by the THERMAL OVERLOAD block. The following briefly describes how the THERMAL OVERLOAD block works, how to program the block, and what adjustments are possible. Each UDC task must contain a THERMAL OVERLOAD block, unless motor thermal overload protection is provided by a hardware device. See J-3676, the Control Block Language instruction manual, for the structure of the block.

CAUTION: Electronic motor overload protection must be provided for each motor in a Distributed Power drive application to protect the motor against excessive heat caused by high currents. This protection can be provided by either the THERMAL OVERLOAD software block or an external hardware device. Applications in which a single power module is controlling multiple motors cannot use the THERMAL OVERLOAD software block and must use an external hardware device or devices to provide this protection. Failure to observe this precaution could result in damage to, or destruction of, the equipment.

The THERMAL OVERLOAD control block is used to create a model of the temperature in a single device, such as a motor or power module, controlled by a DPS drive and to turn on an alarm when an overload condition exists. The block calculates a rise in temperature based on current feedback. When operating above 100%, if the rise in temperature exceeds the programmed limit, the OVERLOAD output will turn on. After the overload condition is detected, the rise in temperature must return to the 100% condition before the drive will be allowed to turn on again.

The operation of the block is programmed through four block input parameters: LIM_BAR, THRESHOLD, TRIP_TIME, and I_FDBK. The value used for LIM_BAR must be the same value entered as the motor overload ratio during drive parameter configuration. The value used for THRESHOLD selects the percent of full load current at which overload is detected. The value used for TRIP_TIME selects the time, in seconds, within which the block must detect an overload after a step from 100% current to LIM_BAR. The main input to the THERMAL OVERLOAD block is I_FDBK. I_FDBK represents current feedback from the PMI in counts (register 211/1211), scaled so that LIM_BAR is 4095 counts.

The main output from the block is OVERLOAD. This boolean will be turned on when a thermal overload is detected. The OVERLOAD output must be programmed in a Ladder Logic task to turn off the drive when the fault is detected. The block also has an output called CALC_RISE. Current feedback is squared, scaled, passed through a Lag fifter, and then written to CALC_RISE.

Consider an example in which LIM_BAR is defined to be 150% of full load current, THRESHOLD is 114%, and TRIP_TIME is 60 seconds. When I_FDBK is at 100%, CALC_RISE will reach a steady state value of 1000, (100% ** 2 / 10). With THRESHOLD at 114%, the trip point for CALC_RISE will be 1300, (114% ** 2 / 10). If I_FDBK is at steady state 100% and then is stepped to 150%, CALC_RISE will integrate up to 1300 in 60 seconds and OVERLOAD will turn on. The OVERLOAD output will stay on until the rise decays to less than 1000. If I_FDBK remains less than 114%, CALC_RISE will remain less than 1300 and OVERLOAD will not turn on.

The rate at which the CALC_RISE block parameter counts up and down is calculated so that a step from 100% to LIM_BAR will turn on the OVERLOAD in TRIP_TIME seconds. If current feedback steps from 100% to a value less than current limit, it will take longer to detect the overload. If I_FDBK is stepped from zero to LIM_BAR, the block will take approximately four times the value of TRIP_TIME to detect the overload.

UL 508C section 56.1.3 specifies that when subjected to 200% of rated full load motor current, the overload protection must trip in at least eight (8) minutes. Because TRIP_TIME is calibrated from 100% to current limit, and TRIP_TIME from zero to current limit is approximately four times longer. the maximum trip time that is allowed is 2 minutes (120 seconds). To meet UL listing requirements, any value greater than 120 seconds is internally limited to 120 seconds.

The National Electric Code (430-32; 1993) requires that thermal overloads protecting motors having a 1.0 service factor trip at load currents no greater than 115% of full load. To meet NEC requirements, the THRESHOLD block parameter has a default value of 114% and should not be set higher.

4.2.2 Local Tunable Variables

A set of local tunable variables with reserved (pre-defined) names is used to store different types of values for use in drive control. For a description of the local tunable variables used in SA3000 drives, refer to Appendix B.

All pre-defined local tunables must be defined in each UDC task (using the BASIC language LOCAL statement) in order for the task to be loaded onto the UDC module. Although all of these variables are not necessarily used in the UDC task itself, they must be defined there in order to provide a reachanism for passing the values between the UDC module and the PMI. For convenience, all these variables are already defined in the UDC task 'skeleton' file in the AutoMax Programming Executive, with "HIGH," "LOW," "STEP," and "CURRENT" values.

Your application task must define these variables using the same "HIGH," "LOW," and "STEP" limit values as the ones found in the skeleton task. Note that you can only change the "CURRENT" value in the application task. If the UDC operating system needs to clamp a value at the higher or lower limit, it changes the actual value in the task and writes error code 958 into the error log for the task.

The local tunable values can be modified through the application task on the UDC module and by the operator using the Monitor function. See the BASIC language instruction manual, J-3675, for more information on local tunable variables and the WRITE_TUNE statement. Local tunable variables cannot be forced.

Like all tunable values in the AutoMax environment, the values of these UDC task tunables are relained through a power loss. Note that the programmer can also define other local tunable variables for application-specific purposes, but the number of local tunables in each UDC task cannot exceed 127.

4.2.2.1 Calculating Local Tunable Values

Depending upon the type of local tunable variable, the "CURRENT" value, i.e., the value to be used for the next scan of the PMI, can be determined in one of the following ways:

1. Self-tune.

The programmer can request the PMI to generate the values for some of the variables. For example, the programmer can set the resolver calibration command bit in register 101/1101 to cause the PMI to adjust the resolver balance.

When the PMI has generated the values, it sends them to the UDC module over the fiber-optic link. The UDC module stores the values in the corresponding tunable variables. A copy of these values is maintained in the PMI for use in the execution of the control algorithm.

2. Tune values from the Programming Executive software and tasks.

The Monitor function in the Programming Executive allows all local tunables to be modified on-line within the limits defined in the LOCAL statement in the UDC task. Note that this is not recommended for the resolver calibration values because these values can be generated more precisely by the PMI during auto-tuning. At the end of the UDC task scan, the new values are sent to the PMI to be used in the execution of the control algorithm. 3. Enter the desired value into the "CURRENT" field for each LOCAL statement.

The programmer can choose to enter the desired values for any local tunables in the "CURRENT" field of the corresponding LOCAL statement or leave them unchanged.

4.2.3 UDC/PMI Task Communication

Coordination between the two PMIs running their respective PMI tasks (drives A and B) and the UDC module running the corresponding UDC tasks is managed through the command and feedback messages sent over the fiber-optic link. The programmer does not control the operating system on the PMI. The timing of the PMI is based on the regulator selected.

A command message is sent to the PMI by the UDC module at the end of every scan of the UDC task. Each message contains the data in registers 100-107/1100-1107, rail data, and the values of the pre-defined local tunables that have changed. Note that some data may be sent over the course of several command messages.

A feedback message is sent to the UDC module by the PMI immediately before the beginning of every scan of the UDC task, i.e., immediately before the CCLK timer expires. Each message contains the data for registers 200-221/1200-1221, as well as any rail data that has changed from the last feedback message.

The exchange of command and feedback register data is synchronized through the use of the constant clock signal (CCLK) on the UDC module as described below. CCLK also enables the coordination of all UDCs in a rack because they will all use the same time base for task execution. Note that all UDC modules in a rack are not required to have the same value in the TICKS parameter of the SCAN_LOOP block in both their tasks. In other words, if the UDC module in slot 6 has TICKS=10 in its tasks, and the UDC module in slot 7 has TICKS=20 in its tasks, the tasks on the UDC module in slot 6 will execute twice as often as the tasks on the UDC module in slot 7, but they will execute on the same time basis, i.e., time zero is determined by CCLK timer expiration.

As soon as the UDC module and PMI are connected over the fiber-optic link, the PMI will request its operating system from the UDC module. Recall that the PMI operating system is part of the UDC operating system. As long as the UDC module has its own operating system and parameter object file, it will download to the PMI the correct operating system.

In order for the PMI and the UDC module to be synchronized, the UDC module must have its operating system, parameter object file, and configuration loaded. In addition, CCLK must be turned on in the AutoMax rack.

If the UDC tasks are already loaded onto the UDC module when the PMI requests its operating system, the UDC module will also send information about when the PMI should send feedback register data required by the UDC task(s). This ensures that the data is measured or calculated as close as possible to the time it is needed in order to ensure it is as current as possible for the next scan of the UDC task(s).

The UDC operating system determines the feedback register message timing required by examining the SCAN_LOOP block in each UDC task so that the leedback will arrive at the UDC module just before it is needed. For example, if the TICKS parameter value in the SCAN_LOOP block were 10, feedback data would be needed by the UDC module immediately before 10 x 500 µsec time expires.

At first, when the UDC module and PMI(s) are powered up and connected via the fiber-optic link, their system clocks are not synchronized. In order for the PMI and UDC module to be synchronized to the same clock signal for communicating command and feedback data on a regular and predictable basis, an AutoMax task must turn on the CCLK signal in the rack. Until CCLK is turned on, command and feedback messages are sent periodically, but not on a predictable basis. CCLK can be turned on by setting the appropriate bit in UDC register 2000 (the interrupt status and control register for both A and B drive tasks), or by setting a bit in another module that can turn on CCLK. Only one module in the rack must turn on CCLK. Note that after a STOP ALL occurs in the rack, CCLK will be disabled and must be re-enabled again in order for UDC tasks to go into run. See figure 4.2 for the typical data flow between the UDC module and the PMI.

To varify that communication between the UDC module and the PMI is resulting in up-to-date feedback data, it is recommended that the drive's run permissive logic include the CCLK synchronized status bit (register 200/1200, bit 14, CCLK_OK@) and the communication lost fault bit (register 202/1202, bit 15, COM_FLT@) as shown below:



Refer to the individual bit descriptions in this manual for more information.

4.2.4 UDC Tasks for SA3000 Parallel Inverters Applications

The SA3000 Parallel Inverters drive uses only one speed loop in the UDC module to generate the torque reference for two PMIs. Each PMI is connected to identical High Power A-C Power Modules, which together provide power to a single dual-wound motor.

One PMI is designated as the primary PMI. It is recommended that this be PMI A. (All of the information presented in this manual regarding \$A3000 Parallel Inverters assumes that PMI A is the primary PMI.) The drive A UDC task contains the speed loop.

The purpose of the drive B UDC task is to:

- Copy the torque reference value (TRQ_REF%) from drive A register 102 to drive B register 1102 (TRQ_REF%).
- Copy the td current feedback value from drive A register 217 (ID_FBK%) to drive B register 1104 (ID_REF%).
- Copy the phase angle data from drive A register 218 (VO_FBK%) to drive B register 1107 (VO_REF%).

All other information presented in this chapter also applies to SA3000 Parallel Inveners applications.



Figure 4.2 - Deta/Time Flow for UDC Module and PMI

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4.3 AutoMax Processor Task and UDC Task Coordination

Recall that all tasks running on AutoMax Processors have access to the UDC dual port registers, but that UDC tasks can only access those common variables that represent registers in their own dual port memory. Task coordination between the UDC module and the AutoMax Processor is generally handled through periodic hardware interrupts generated by the UDC module. An AutoMax task needs to define a hardware "event" that will trigger some action by an AutoMax task, using the BASIC statement EVENT. The EVENT statement must reference the hardware interrupt status and control register ISCR% (register 2000 in the UDC dual port memory).

Although the UDC operating system itself actually causes the interrupt, a task in the rack (AutoMax or UDC) must write to the scans per update register in the UDC dual port (register 2001) in order to define the number of UDC task scans between updates of the the Nth scan application registers (1300-1599), and between hardware interrupts. Sce figure 4.3 for more information.

Note that the register values being latched on every Nth scan provide a consistent context for evaluation of Control Block statements, but that BASIC statements in UDC tasks read and write data immediately; that is, they do not read from and write to a local buffer. Referencing the same common values in both Control Block and BASIC statements in one task can result in errors.

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Figure 4.3 - Nth Scan Interrupts



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5.0 ON-LINE OPERATION

DANGER

ONLY QUALIFIED ELECTRICAL PERSONNEL FAMILIAR WITH THE CONSTRUCTION AND OPERATION OF THIS EQUIPMENT AND THE HAZARDS INVOLVED SHOULD INSTALL, ADJUST, OPERATE, OR SERVICE THIS EQUIPMENT. READ AND UNDERSTAND THIS MANUAL AND OTHER APPLICABLE MANUALS IN THEIR ENTIRETY BEFORE PROCEEDING. FAILURE TO OBSERVE THIS PRECAUTION COULD RESULT IN SEVERE BODILY INJURY OR LOSS OF LIFE.

The ON LINE! command in the System Configurator and the Task Manager applications allows you to access options such as leading, running, and monitoring tasks in the rack. All of the options are described in detail in the AutoMax Programming Executing Instruction manual.

The following sections provide a summary of some of the options as applied to the UDC module and UDC tasks. Note that you must load operating systems onto the Processor modules and UDC modules in the rack before attempting to use any of the on-line options.

5.1 Loading the UDC Module's Operating System

Like the AutoMax Processor, the UDC module requires an operating system. You can load the operating system to a UDC module by using the Load Operating System command from the Command menu in the System Configurator. Refer to the AutoMax Programming Executive instruction manual for the procedure. You must load the operating system(s) to the AutoMax Processor(s) at the same time or before you load the UDC module operating system.

You have the option of loading the operating system to the UDC module in a slot you specify or to all UDC modules in the rack. It is possible to re-load a single UDC module's operating system without having to re-load the operating systems to all of the UDC modules in the rack.

The leftmost AutoMax Processor in the rack will check for compatibility between the AutoMax operating system and the UDC operating system. If you replace a UDC module with another UDC module that already contains an incompatible operating system, the new UDC module will be disabled and its "OS OK" LED will be turned off.

5.2 Loading the Drive Parameters and UDC Tasks

The drive parameters specified when the UDC module is configured can be thought of as the UDC configuration. Like the AutoMax Processor, the UDC module must have its configuration loaded before it can execute any tasks. You can load the drive parameters and UDC tasks to the UDC by selecting "L" for Load from the ON LINE Transfer menu. Several options, which are briefly described before, will be displayed on the screen.

You have the option (By selecting "A" for All) to automatically load the rack (i.e., AutoMax Processor configuration, the drive parameters for all the UDC modules in the rack, and all tasks for the rack (including all UDC tasks).

You have the option of loading the drive parameters to the UDC module in a slot you specify or to all UDC modules in the rack. When the drive parameters are loaded, the AutoMax Programming Executive will determine if the drive parameters are compatible with the existing rack configuration. If the drive parameters are not compatible, an error message will be displayed on the personal computer.

You also have the option of loading UDC tasks to the UDC modules in the rack. If you choose to load tasks, the Programming Executive will display a list of all the AutoMax tasks and UDC tasks for the system. Select the task you want to load from the list. Remember that you must load the rack configuration and the drive parameters before loading UDC tasks to a UDC module.

Refer to the AutoMax Programming Executive Instruction manual for the complete Load procedure.

5.3 Running, Stopping, and Deleting UDC Application Tasks

WARNING

UNDERSTAND THE APPLICATION BEFORE STARTING A TASK. OUTPUTS MAY CHANGE STATE, RESULTING IN MACHINE MOVEMENT. FAILURE TO OBSERVE THESE PRECAUTIONS COULD RESULT IN BODILY INJURY.

WARNING

IT IS THE RESPONSIBILITY OF THE USER TO ENSURE THAT THE APPLICATION PROCESS STOPS IN A SAFE MANNER WHEN THE APPLICATION TASKS STOP, FAILURE TO OBSERVE THESE PRECAUTIONS COULD RESULT IN BODILY INJURY.

Running UDC Tasks

A UDC application task is required in order to control a Distributed Power drive. To control two drives, two UDC tasks are required. Once it is loaded to the UDC, a UDC application task is included in the on-line task list with the AutoMax Processor application tasks. It can be run, stopped, monitored, or deleted in the same way as any other application task. The priority field will be set to "N/A" for UDC application tasks. The task for drive A always executes first, followed by the task for drive B.

The Run All command will run all AutoMax and UDC tasks. The UDC module's tasks can be run whether or not the following conditions are mot:

- the PMI is communicating with the UDC module
- the PMI operating system has been loaded from the UDC module to the PMI (which happens automatically when the PMI is connected to the UDC module)

Stopping UDC Tasks

UDC applications tasks (both tasks A and B together) must run a least every 10 milliseconds. Once the SCAN_LOOP statement is executed, the UDC module will cause a Stop All in the rack if the task does not complete its scan within 10 milliseconds.

Deleting UDC Tasks

When a UDC application task is deleted, any local variables which were forced are removed from the force table. The task's error log is also cleared.

5.4 UDC Information Log and Error Log

The information log and the error log for a UDC task can be displayed by selecting "I" for Info/Log from the ON LINE menu. Refer to the AutoMax Programming Executive for the procedure.

The Information log for a slot containing a UDC module will display the UDC operating system's part number, the utilization of the CPU resources in the UDC module, and various memory and PMI rack statistics. Select "U" from the fnfo/Log menu to display the information log. Note that the UDC module's CPU utilization should not exceed 75%.

Like AutoMax tasks, UDC tasks can also access the error log by using the BASIC statement CLR_ERRLOG@ and BASIC function TST_ERRLOG@. The error log will display the first, second, and last errors and will maintain them until power is cycled.

Appendix A

SA3000 Drive Register Reference

	REGISTER MAP	UDC-PM	COMMUNICATION STATUS		FEEDBAH	CK REDISTERS	
Registers	Function	A/6 00/1000	UDC mitch: a profistations	10	6/8		
i i care e c		9034900	HI		200/1200	Drive status	
0-21	den sea por regiones		 If weaks now indemaph If we out of leaves year 	10 A		Bt	734 0440
24-78	System Use Only		2 CPGTaming pro:			1 Ceins calculated	PMI ATCH
80.39	DCPWI ochm. status registers for drive A		5 Overnin error			2 Traj ref set plus	THE EPS
90-59	Bysten Use Only		4 DWA tomatienter 5 Tonon ter under und			4 D C bus ready	BUS RIVE
100-108	Command registers for drive A		8 CCLK comm synch -	erver		5 Constant bet region - Steater wind CK	PWR_RNGP
107-198	System Use Only		7 Enopback data error	(m)		8 Fault detected	FITS
200-222	Feesback registers for citye A		9 Multipleted data ve	Featier to lare		9 Warring detected 14 CELK synchrol 4 Witto LEE	WING HOULK DREE
223-299	System Use Only		10 No match ng PM C6			ts PMI OE maded	PNI OK2
300 590	Application registers updated every scan- for orives A and B	94 1 4034	11 Invalid PVII OS failed 12 Incompatible PVII H/ UDC conduct according	er W	201/1201	All sinitas 14	
600-399	System Use Only	A>/ 1031	SDC module CRC error	court		DE la percisaria laput	FF 122
1000	JDC module test switch register	85/1053	UDG module formatient	r count		1 M-contactor stok mout	M_FCBKW
1011-1017	 CDC module merer port astap registers 	84/1034	PM pensials			2 115VAC succinged 2	ALX NLS
10:8-1075	System Use Only		0 invalid as internati			3 154AD and input 3	ALK IVSG MIN ISLAS
1090-1099	UDC/PIN commissions registers for drive 9		 Diriend of itame state OCOL 	115		5 15WAC aux input 5	ALK Nov
1080-1080	System Use Only		2 Collaboring and 3 Overun error			SRuskr gen calls complete 2 Boskr bal calls complete	RES GANS
1100-1100	Command registers for draw 15		< DMA formati error			S Baemal st-obe detected	STR_DED3
1107-1185	System Use Only		5 Innen her utderter 8 CC Communication	1		9 Baemai si ola ievel 19 STATORI, Zinne complete	TUNED 122
1903-129-	Fredback recision to only B		8 VDC CCLK comm s	moh error	2061202	Drive Bult	2005/20078
1292 1265	System like Only		R Multiple and state wet	Collies before		31	
1300 1595	Application registers updated every Nm scan for drives A and B		12 Invalid PVE start Ds 13 Insuit, PVI memory 1 14 Invalid PVI, raat add	b load PNI OS		90 C bus over voltage 10-C bus over surrent	
1800-1993	Bystem Use Only	1000	15 PM: OS over low	999 - C		2 Compare current fault 3 Instantionecus men current	FU KONS
2005-2010	Inter-up Blat, s and Control repisters for	85/1035	PM good mag, reckill o PM DEC arms on at	Courts		4LP-macule list.	FUT UPING
1020055	shrives A and B	87/1037	PM formal error count			SCharperta, et me-out	FUT CHUG
2011-2047	" Şyrdəm Baa Only	65/1038 69/1018	i – Commy ink status UDC transmitted meg. o	t-m		7 Ocer temperature (aut. 5 Resolver bruken wirk 9 Resolver mot de fauit 20 Ocer source (aut.	FU DT& FU IBAAS FU IBAAS FU IBASS
	REGISTER/BIT DESCRIPTIONS	COMMANA A/B	ID NEGISTENS			11 Perser Technology foult 12 PMI person supply foult 13 PMI bas (cult	FUT_PTWA FUT_PSQ FUT_PLSA
RAIL NO P	TORT RECUBIERS	100/ 100	"low control			15 PM communication for:	FU_COMS
			31 		2031205	Drive warring	304230353
5/6	but the second		 Enable minoripab Enable minoripab 	TROUND		31	
118	FWI por 0, channel 1		2 Eneck, priego test.	BRG TET D		20-0 bus ever voltage	WAN OWE
2/14	FMI poin 0, oher not 2		4 Enable bus	BUS_ENAR		1 D-C bus under voltage 2 Ground current warning	WAN ISNDER
8/15	FMI port 0, phannel 3		5 Vector align request 5 Fact areas	ELT DSTOO		3 Voltage rtople warning	Way Arth
-116	FMI ponie raute jseo belowy EMI ponie ocerek bu fau Loculture		9 Watching reset	WEN FETO		< Reference in Emil STublen abrides	WHY DUNE
6/18	FMI port 1, shannel 0		10 Enable parallel PM A	PFM_EWAS		SLose steining warming	WAN SHEET
7.19	FWI pon 1, phannel 1		11 Enable parallel PM R	PFW_FVRg		7 Over temperature warning 6 Sectorem mater	WAY DISA
8720	FMI port 1, channel 2		12.1 mages cars let + to 1. 15.11.10 tank microsom Magned	7 OCC FUND		19 Austr was senatu	WAN YONS
0.721	PNI por 11 channel 3			dans loants		saat mei Reffist	WAN FAME
11/22	Philippint and size accord	10.7° 101	C Colug			15. Eal techanication error 14 COUK net synchronized	WAN RADS
00.074			B1			15.5% communication amor	WRN_COMM
	Pal Fault Bits		4 Automity Calgul	AUXOJIA	204(1204	Prover device publics	
	C. Contractor II in and managements		6 Enable is we call that	RES_CALO		III	
	A deg on 0 input utdevrance		2 Enable esternal strate	STR ENAD		D Phase U-upper LDC A	STARE O
	2 Arizing on, 1 input overrange		10 Erich STATCS Zourn	TI NE 155		2 Phase Wupper IDE A	W JEAD
	8 Analog of 1 input under range		15 UGC pert loopback test	UCC LING		S Phase U lower IOC A	U_LOAS
	 Analogieh 2 inpla overrange 	1022 102	Terrare selections	TEO BES		4 Phase Viewer IDC A	V 1043
	 Andlog on, 2 input under range Andlog on, 2 input under range 	10.11. 104	B entresse	ELX BEEN		6 Intelligent Per Midl A lauft	IF MAD
	 Andogion, Simple overlangs Andogion, Simple under range 	104"104	la reference	ID_REFS		7GD ta.kA	GDI42
	8 No covice plugged into configured part	105' 105	Di dre lesi ocde	TST CODES		B BLS charge time-a.1 A 12 Over tomperature A	CINER
	9 Bad IC coue	1002.104	PSt 2% guident	PTI DAS		18 Phase U surrent sharing A	U_S (842)
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Appendix A

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15 Phase Weaters sharing B. W_SHPE(V)

SA3000 Local Tunable Variables

Current Minor Loop Gain Variables

The stator resistance and the stator time constant values can be generated automatically by using the enable tuning command in register 100/1100. The values generated by the system should not require adjustment. If any of these values are modified outside of acceptable limits, the new value will be ignored and the last acceptable value entered will be used. Bit 8 in warning register 203/1203 will also be set to indicate the value entered was invalid.

CML_WCO% - Current Minor Loop Crossover Frequency

Default Current Value: 1000 Low Limit: 1000 High Limit: 4000 Step: 1

The value in this variable selects the desired response of the current minor loop. The higher the value, the more quickly the drive responds to a change in forque reference current. Note that if the value is adjusted too high, the current minor loop will become unstable. This value is entered in radians/second.

STATOR_R_E4% - Stator Resistance

Default Current Value: 1 Low Limit: 1 High Limit: 10000 Step: 1

The value in this variable is used to adjust the gain of the current minor loop. It is also used in flux teadback calculations. It is the resistance of the stator. It is entered in ohms times 10000. For example, a resistance of 0.1 ohms is entered as 1000.

STATOR_T_E4% - Stator Time Constant

Default Current Value: 1 Low Limit: 1 High Limit: 10000 Step: 1

The value in this variable is used to adjust the gain of the current minor loop. It is the time constant of the stator. It is entered in seconds times 10000. For example, a time constant of 50 msec is entered as 500.

FLX_WCO% - Flux Loop Crossover Frequency

Default Current Value: 10 Low Limit: 5 High Limit: 50 Step: 1

The value in this variable is used to adjust the bandwidth of the flux loop used in the Constant Power version of the \$A3000 Vector regulator. It is entered in radians/second where 1=1 radian.

Continued

Vector Algorithm Gain Variables

The vector algorithm gain variables are used to adjust the gain of the vector control algorithm. The no load stator current variable can be generated automatically by using the enable funing command in register 100/1100. The value generated by the system should not require adjustment. If this value is modified outside of acceptable limits, the new value will be ignored and the last acceptable value entered will be used. Bit 8 in warning register 203/1203 will also be set to indicate the value entered was invalid.

STATOR_IZ_E1% - No Load Stator Current

Default Current Value: 0 Low Limit: 0 High Limit: 8486 Step: 1

The value in this variable represents the amount of magnetizing current (flux). It is entered in ampsitimes 10. For example, a no load stator current of 10 amps is entered as 100.

Verifying STATOR_IZ_E1% When Using High Slip Motors

The value in local tunable STATOR_IZ_E1% (no load stator current) is generated automatically by the system by setting the Enable Tuning bit in the Drive Control register (register 100/1100, bit 1, PMI_TUN@). However, if you are using a high alio motor, the value calculated for this variable may not be correct. It is important that you verify the value in this variable using the following procedure if you are using a high slip motor.

- Step 1. Command the motor to its synchronous speed with no load. Synchronous speed in RPM = 120 x fo/no. of motor poles, where fo = rated motor frequency in hertz.
- Step 2. At synchronous speed, monitor motor voltage using register 209/1209.
- Step 3. Modify the value in STATOR_IZ_E1% until motor voltage is approximately 97% of rated motor voltage.

Example:

The following example applies the above procedure to verify the value of STATOR_IZ_E1% for a 60 Hz, four-pole high slip motor with a rated motor voltage of 460V, a rated speed of 1755 RPM, and rated full amps at 11.9 amps.

- Step 1. Command the motor to its synchronous speed with no load Synchronous speed = 120 x 60 / 4 = 1800 RPM Command = (1800/1755) x 4095 = 4200 counts.
- Step 2. At synchronous speed, monitor motor voltage using register 209/1209.
- Step 3. Modify the value in STATOR_IZ_E1% until motor voltage is between 427V and 435V. The higher value is preferred.

Tuning STATOR_IZ_E1% for Constant Power Applications

For constant power applications (i.e., Constant Power is selected on the Motor Data screen), use the following procedure to calculate the value for STATOR_IZ_E1%:

- Stop 1. Sot bit 1 in register 100/1100 (Enable Tuning) to one to request the PMI Processor to calculate the local tunable values. When the calculations have been completed, the system will set bit 1 in register 200/1200 (Automatic Tuning Complete) to one.
- Step 2. Set bit 1 in register 100/1100 to zero.

Continued

- Step 3. Command the motor to 70% of its synchronous speed with no load. Synchronous speed in RPM = 120 x fo/no. of poles, where fo = rated motor frequency in hertz.
- Step 4. With the motor at synchronous speed, set bit 10 in register 101/1101 (Enable STATOR_I2_E1% Tuning) to one. The system will tune the value in STATOR_I2_E1% and set bit 10 in register 201/1201 to one when the value in STATOR_I2_E1% has been successfully tuned.
- Step 5. Set bit 10 in register 101/1101 to zero.

NOTE: If the system is unsuccessful in tuning the value for STATOR_IZ_E1%, it will set bit 5 in register 203/1203 (Tuning Aborted Warning). This can occur if the motor speed is less than 50% of synchronous speed, the motor speed is greater than or equal to 80% of synchronous speed, or the magnetizing current is still in saturation at that speed.

SLIP_ADJ_E3% - Slip Adjustment

Default Current Vatue: 850 Low Limit: 500 High Limit: 1500 Step: 1

Rotor slip is calculated automatically by the system. The value in this variable is used to adjust the resulting rotor slip value. As this value is increased, higher stator frequency is produced. Note that slip may vary with rotor temperature. This value may be changed through an application task to compensate for temperature changes. A value of 1060 corresponds to a gain of 1.000.

D-C Bus Variables

The programmer selects the values in the following variables to determine the drive's response to changes in the D-C bus. Note the following relationship must be true or a drive warning will be generated (register 203/1203, bit 8): PLT_E0%<UVT_E0%<OVT_E0%, For more information about internal D-C bus control, refer to the appropriate SA3000 Power Modules manual.

OVT_E0% - Over Voltage Warning Threshold

Default Current Value: 300 Low Limit: 300 High Limit: 1000 Step: 1

A drive warning is generated (203/1203, bit 0) if DC bus voltage exceeds the value stored in this variable. It is entered in volts. This value should be set below the hardware over voltage fault limit (900V for Medium Power A-C Power Modules; 925V for High Power A-C Power Modules) and above the normal operating voltage (displayed in the D-C Bus Voltage feedback register (206/1206)).

This value also selects the starting point at which the system begins reducing the regeneration torque limit. Bit 4 of the Drive Warning register (203/1203) is also set to indicate the system is limiting torque.

UVT_E0% - Under Voltage Warning Threshold

Default Current Value: 250 Low Limit: 250 High Limit: 825 Step: 1

A drive warning is generated (203/1203, bit 1) if D-C bus voltage is less than the value stored in this variable. It is entered in volts. This value should be set above the value selected for the Power Loss Threshold variable.

Continued

This value also selects the starting point at which the system begins reducing the motoring torque limit. Bit 4 of the Drive Warning register (203/1203) is also set to indicate the system is limiting torque.

PLT_E0% - Power Loss Fault Threshold

Default Current Valu	Đ:
Low Limit: 250	
High Limit: 825	
Step: 1	

A drive fault is generated (202/1202, bit 6) if D-C bus voltage drops below the value stored in this variable. This value should be set to 100V below the normal operating voltage of the bus (displayed in the D-C Bus Voltage Feedback register (206/1206)). It is entered in volts.

VRT_E0% - Voltage Ripple Warning Threshold

250

Default Current Value: 14 Low Limit: 10 High Limit: 16 Step: 1

A drive warning is generated (203/1203, bit 3) if ripple (voltage variation) on the D-C bus exceeds the value stored in this variable. This diagnostic is operational after the bus has reached steady state. This is intended to be used to detect an input phase loss in the converter section if a three-phase A-C input is used, however this can also be used with a common bus supply. It is entered in volts. When deciding what value to use for PLT_EO%, recall that the instantaneous change in voltage on the bus capacitors in the Power Module cannot exceed 100V.

Resolver Gain and Balance Variables

The resolver gain and balance variable values are used to compensate for varying lengths of resolver wiring. The balance value can be generated automatically by commanding the resolver calibration test in register 101/1101. The gain value will be generated automatically when the RES_GAN% variable is equal to zero, i.e., on power-up. Refer to the Power Module Interface Rack manual for more information on the calibration procedures.

Note that the Distributed Power Systems are designed to be used with the Reliance resolvers described in the PMI Rack manual. The validity of the results of these calibration procedures are not guaranteed if resolvers other than those described are used.

RES_GAN% - Resolver Gain

Default Current Value: 0 Low Limit: 0 High Limit: 255 Step: 1

When the value in RES_GAN% is equal to zero, the gain tuning procedure is performed automatically by the operating system. The default CURRENT value is 0. The value ranges from 0-255 counts, with 1 count representing .15 volts of gain. It is recommended that this value be generated using the auto-tuning procedure because the PMI Processor can take into account the entire resolver circuit when setting the proper gain value. If the value is adjusted too low, a drive fault will be generated (registor 202/1202, bit B). If the gain needs to be re-calibrated, reset the value of RES_GAN% to zero. However, do not reset the value of RES_GAN% to zero while the inner loop is running {i.e., TRQ_ON@ is set) or a drive fault will be generated (register 202/1202, bit 8).

Continued

RES_BAL% - Resolver Balance

Default Current Value: 0 Low Limit: 0 High Limit: 79 Step: 1

The RES_BAL% local tunable contains the value of the resolver balance, i.e., the amount of capacitance (in pF) that is to be added to the sine or cosine channel of the resolver to compensate for wiring. Valid values are from 0 to 79, with 0 representing the fact that balance tuning has not been performed. Values from 1 to 39 add capacitance to the cosine channel, while values from 41 to 79 add capacitance to the sine channel. Each integer value represents 100 pF as shown in figure 8.1.



Figure B.1 - Capacitance Used for Resolver Balancing

Diagnostic Variables

The programmer enters the values in the diagnostic variables to establish thresholds at which drive warnings are generated.

GIT_E1% - Ground Current Warning Threshold

Default Current Value: 100 Low Limit: 10 High Limit: 2000 Step: 1

A drive warning is generated (203/1203, bit 4) if ground current exceeds the value stored in this variable. This value should be set above the value in the ground current feedback register (208/1208) after the drive is operational, it is entered in amps times 10. For example, 50.1 amps is entered as 501.

IST_E1% - Current Sharing Warning Threshold

Default Current Value: 600 Low Limit: 10 High Limit: 2000 Step: 1

A drive warning is generated (203/1203, bit 6) if the motor output current is less than the value stored in this variable. This variable is only used when High Power A-C Power Modules are connected in parallel. It is entered in amps times 10. For example 50.1 amps is entered as 501.

Appendix C

SA3000 Control Algorithm

SA3000 drives and SA3000 Parallel Inverters regulate current (torque) to A-C motors using a vector regulation algorithm. (In SA3000 drives, the output of drive A controls the drive A motor, and the output of drive B controls the drive B motor. In SA3000 Parallel Inverters, the output of drives A and B are locked together to control one motor.) This algorithm, also referred to as a minor loop or a regulator, is described below and illustrated in the block diagrams on the following two pages.

The UDC application control task passes the torque reference command in TRO_REF% (102/1102) to the PMI, where a value of +/-4095 corresponds to the motor overload ratio amps specified for the motor in parameter configuration. For SA3000 Vector and Constant Power drives, drive A and drive B each receive their torque reference from separate speed loops in the UDC module. For SA3000 Parallel Inverters, there is only one speed loop supplying the same torque reference to both drive A and drive B.

in vector control, the motor currents are separated into two components, Iq and Id. The Iq component produces the torque in the motor while the Id component is the magnetizing current which produces the flux in the motor.

The Id component is normally calculated by the PMI Processor based on the no-load stator current configuration parameter entered by the programmer. (For SA3000 Parallel Inverters, Id is calculated only in the primary PMI.) The programmer can select to calculate Id in the UDC task instead in order to operate the motor at speed ratios up to 2:1 (motor speed/base speed) or to control the flux directly. For constant power operation at speed ratios up to 4:1, the programmer can select to have the PMI calculate the value of Id using integrated motor voltage feedback. The vector algorithm combines the Id and Iq components to produce a vector that is equal to the total current required by the motor to produce the desired torque.

The vector algorithm calculates the electrical phase position of the current reference. This is determined from the ld and lq reference vector, the motor speed feedback, and the slip calculation. The outputs of the vector algorithm are three current reference signals, one for each phase of the motor.

These current reference signals are compared with the current feedback signals, producing error signals which feed proportional + integral function blocks. The output of these blocks is a voltage reference. The voltage signal is further conditioned by a harmonic injection signal designed to reduce the harmonic content of the drive's output. The conditioned voltage reference is then compared against a triangle wave. The output of the comparator block is a PWM waveform, which drives the power devices in the inverter bridge to pass current to the motor.



SA3000 Vector Algorithm Block Diagram



Appendix C





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Appendix D

Status of Data in the AutoMax Rack after a STOP_ALL Command or STOP_ALL Fault

	AutoMax Processor	UDC Module	PMI Processor
LOCAL tunable variables	retained	retained	retained
LOCAL variables	retained	reset to 0	N/A
COMMON memory variables	non-volatile are retained; others are reset to 0	N/A	N/A
I/O variables (including UDC dual port memory)	inputs retained and updated; outputs are reset to 0	see below	all I/O is reset to 0
Input values, including: Feedback registers UDC/PMI communication status registers UDC Error Log Info	retained	retained	N/A
Output values, including: Command registers Application registers ISCR registers Scan-per-interrupt register Scans-per-interrupt counter	reset to 0	reset to 0	N/A
Parameter configuration variables	N/A	relained	N/A
UDC test switch information	N/A	retained	N/A
D/A setup configuration	N/A	retained	N/A
Operating system	retained	retained	ratained

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Appendix E

Torque Overload Ratio Parameter Precautions

The maximum RMS current that will be generated by the Power Module based on the Torque Overload Ratio ontored must be within the limits of the selected Power Module or a warning will be generated. In some cases, however, the internal limit checking rules may be too conservative and generate a warning even when the Power Module Rated Current and Torque Overload Ratio values are consistent.

Internal limit checking for this parameter cannot be performed more accurately because the magnetizing component of the current (iz) is not available until tuning is enabled in the PMI. Tuning, in turn, cannot be performed until the parameter object file and UDC task have been loaded to the UDC.

To determine the specific value of maximum RMS current that can be supplied by the Power Module at a given Torque Overload Ratio level, use the following equation. If the result is less than or equal to Power Module Rated Amps (at the selected carder frequency), you can ignore the warning.

Maximum RMS Current = Square root of [(Torque Overload Ratio/100)² x (Rated Motor Current² – $|z^2$)] + $|z^2$]

Where Iz is the magnetizing current component of the Power Module output. Iz is stored in tunable variable STATOR_IZ_E1%. The value for this variable can be generated by enabling tuning in register 100/1100, bit 1. Note that you must load a complete parameter object file and UDC task to the UDC module before you can enable tuning.

Appendix F

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The VDC Input Range and Carrier Frequency Limit for Each SA3000 Power Module

Power Module Part Number	VDC Input Range	Carrier Frequency Limit
B05412-26 (14A @ 2 kHz) 776 VDC in	310 - 900	2-8 kHz
805412-24 (17.5A @ 2 kHz) 621 VDC in	310 - 800	2-8 kHz
805412-36 (28A @ 2 kHz) 776 VDC in	310 - 900	2-8 kHz
805412-94 (95A @ 2 kHz) 621 VDC in	310 - 800	2-8 kHz
805412-6 (56A @ 2 kHz) 776 VDC in	310 - 900	2-8 kHz
805412, -1, -2, -3 (70A @ 2 kHz) 480 VAC in	310 - 800	2-8 kHz
805412-4 (70A @ 2 kHz) 621 VDC in	310 - 800	2-6 kHz
805412-6 (112A @ 2 kHz) 776 VDC in	310 - 900	2-8 kHz
805413, -1, -2, -3 (140A @ 2 kHz) 460 VAC in	310 - 800	2-8 kHz
805419-4 (140A @ 2 kHz) 621 VDC in	310 - 800	2-8 kHz
805414, -1, -2, -3 (240A @ 2 kHz) 460 VAC in	310 - 800	2-8 kHz
805414-4 (192A @ 2 kHz) 776-800 VDC in	310 - 900	2-8 kHz
805414-4 (240A @ 2 kHz) 621 VDC in	S10 - 800	2-8 kHz
803430-S (534A @ 2 kHz) 776 VDC in	310 - 925	4 kHz
803430-T (972A @ 2 kHz) 776 VDC in	310 - 925	4 kHz
803430-V (1457A @ 2 kHz) 776 VDC in	\$10 - 925	4 kHz
W/D 30395-11 (534A @ 2 kHz) 776 VDC In	310 - 925	4 kHz
W/D 30395-12 (972A @ 2 kHz) 776 VDC in	310 - 925	4 kHz
W/D 30395-13 (1457A @ 2 kHz) 776 VDC in	310 - 925	4 kHz

Appendix G

Constant Power Parameter Entry Example



Appendix H

New Features in Version 1.2

The SA3000 Version 1.2 software includes support for SA3000 Parallel Inverter drives.

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Reliance Electric Documentation Improvement Form

Publication Name: Publication Number:	Publication	Publication Date:	
Use this form to give us you have found. For convenience you have completed this for	or comments concerning this publicate, you may attach copies of the pay rm, please return it to:	ition or to report an error that you ges with your comments. After	
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