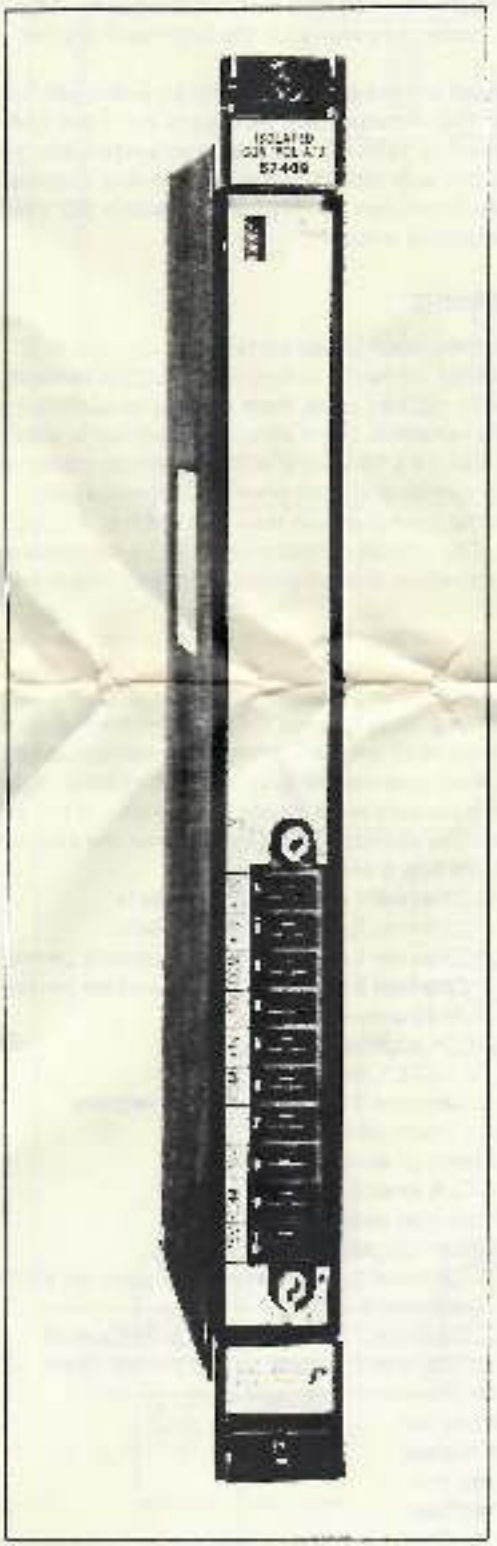
Isolated Control A/D Module
57409



Reliance Distributed Control System

Features

Two input channels
±1V or ±10V input ranges
12-bit conversion plus polarity
100% overrange capability
500V isolation between inputs and logic
Software selectable input filtering
Software settable sampling rates
Constant clock (CCLK)
Interrupt capability
Precision voltage source for potentiometers
Usable in a Main Rack or Remote Rack

Function

The Isolated Control A/D Module provides for input to the Distributed Control System (DCS) of variable D-C reference or feedback signals for high performance closed loop control. It can also be used as a general purpose input for analog signals that are less time-critical.

Mechanical Description

The Isolated Control A/D Module is a printed circuit board assembly that plugs into the Multibus® backplane of the DCS Rack. It consists of the printed circuit board, a faceplate, and a protective enclosure. The assembly dimensions are listed under "Technical Specifications."

The faceplate of the module contains a P3 female connector socket. External signals are connected to this socket via a supplied multiconductor cable with an attached 10-point terminal board plug. The socket and plug are keyed to prevent insertion of the cable plug into the wrong module.

Also on the faceplate are four LED indicators. The top two LEDs indicate that CCLK is on and that CCLK is enabled from this module. The lower LEDs are for factory testing.

The standard connectors that interface with the system Multibus are at the back of the module.

Electrical Description

The circuitry in the module is divided into two sections, the isolated input circuits and the digital logic circuits. The two sections are connected by five optical isolators and a DC-to-DC isolated power supply. A block diagram of this circuitry is shown in Figure 1.

Isolated Input Section

Input scaling amplifiers are designed for ± 5 mA input for

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full-scale conversion to ±4095. Resistors are provided on the PC board for inputs of ±10 volts or ±1 volt full scale. Other inputs can be accommodated by connecting resistors to the terminal board as shown. The PC board resistors are rated at ½ watt.

Low pass filters with software selectable bandwidths smooth out transients and also provide anti-aliasing for signals with high frequency components. The two-pole filters have a damping factor of .75 with corner frequencies (90-degree phase shift) listed under "Programming."

Sample-and-hold circuits maintain constant input values during conversion. A multiplexer selects the channel to be converted.

A gain switch reduces the gain between the input signal and the successive approximation comparator when the signal exceeds the nominal input value. When in this overrange condition, conversion accuracy is degraded and there may also be a discontinuity during the transition. Thus, the overrange should only be used to detect abnormal signal levels. (Maximum overrange converts to ±6191.)

A precision voltage source provides the reference signal for the successive approximation digital-to-analog converter. Reference polarity is switched for negative input signals to provide the full 12 bit conversion in either polarity. The inverted gain is factory adjusted to make the positive and negative references equal in magnitude. The output of the D/A converter is compared with the input signal as each bit is tested in descending order during the successive approximation conversion routine.

Latches are used to store serial data from the digital logic section and convert it to the parallel data required for the filter selection and for the D/A converter.

Digital Logic Section

The Multibus interface is similar to all other DCB modules. The module's location is identified by module address ID lines on P2. On receipt of a memory read or memory write signal from a Processor Module, the module and register address lines are decoded, and data is transferred between the Multibus data lines and one of the eleven registers of onboard memory. A transfer acknowledge signal is returned to the Processor. Upon powering up, control and status registers are set to zero by the initialize or board reset signal but not the data registers. The control and data register definitions are listed under "Programming."

This module contains a 4 MHz clock that can be used as the Multibus constant clock (CCLK). Whether or not it is used is determined by a software settable control bit. Only one CCLK can be enabled in a rack. This must be done after the filter frequency is selected and the update period is set on all Isolated Control A/D Modules in the rack and after similar registers are set on all other modules that use CCLK.

The CCLK signal is divided by four to produce a 1 MHz signal for timing the successive approximation conversion. It is further divided to produce a signal (TIK) every 500 microseconds that initiates a conversion cycle for both input signals or causes the filter selection to be updated on either or both channels if changed.

The local bus control includes the functions of update period counters for each channel. When the CCLK is enabled, the value in the preset count register of local memory for each channel is transferred to the respective current count register. At each 500 microsecond TIK signal, each current count register is decremented by one count. When either register reaches zero, the latest input value for that channel is transferred to the respective input data register, and the current count is reset to the preset value. This can also generate an interrupt to the Processor Module if programmed to do so.

If the preset count register is set to one, the input data register will be updated every 500 microseconds. This is the normal mode of operation if the interrupts are not used.

The interrupt drivers are enabled by an event definition statement in the software task that reads the input channels. When the event is defined, the operating system assigns it an interrupt line and identifies the module and channel that drives it. There can be up to four possible I/O interrupt sources defined on a rack.

Programming

The software required to use an Isolated Control A/D Module consists primarily of defining a logical variable name for each register used, then reading or setting the values of the variables. If the interrupt function is used, there must also be a hardware event definition statement. The variable names and their physical addresses are assigned in the configuration task in IODEF or RIODEF statements. The logical names must also be declared as COMMON variables in each application task that refers to them.

Isolated Control A/D Module registers are defined below. Undefined bits either are not used or are for manufacturing test purposes only. Values must always be assigned to registers 7, 8, 9, and 10 before the CCLK is enabled. Registers 0 through 4 are read only; all others are read/write. To turn on the CCLK on a particular module, bit 6 of both registers 5 and 6 of the module must be set true by one of the application tasks. The application tasks can read the status of the CCLK from bits 6 and 8 in register 4.

Register 0: Channel 1 converted input data
Register 1: Channel 2 converted input data
Register 2: Channel 1 current count of update period
Register 3: Channel 2 current count of update period
Register 4: Read only status
  Bit 6 - CCLK enabled
  Bits 8, 10 - CCLK on
Register 5: Channel 1 interrupt control register
  Bits 0, 1 - Interrupt line ID
  Bit 2 - Interrupt allocated
  Bit 6 - CCLK enable
  Bit 7 - Interrupt enabled
  Bit 15 - Interrupt device flag
Register 6: Channel 2 interrupt control register; same as register 5
Register 7: Channel 1 update period preset count
Register 8: Channel 2 update period preset count
Register 9: Channel 1 filter selection
  0 = 300 rad/sec
  1 = 145 rad/sec
  2 = 79 rad/sec
  3 = 21 rad/sec
Register 10: Channel 2 filter selection; same as register 9

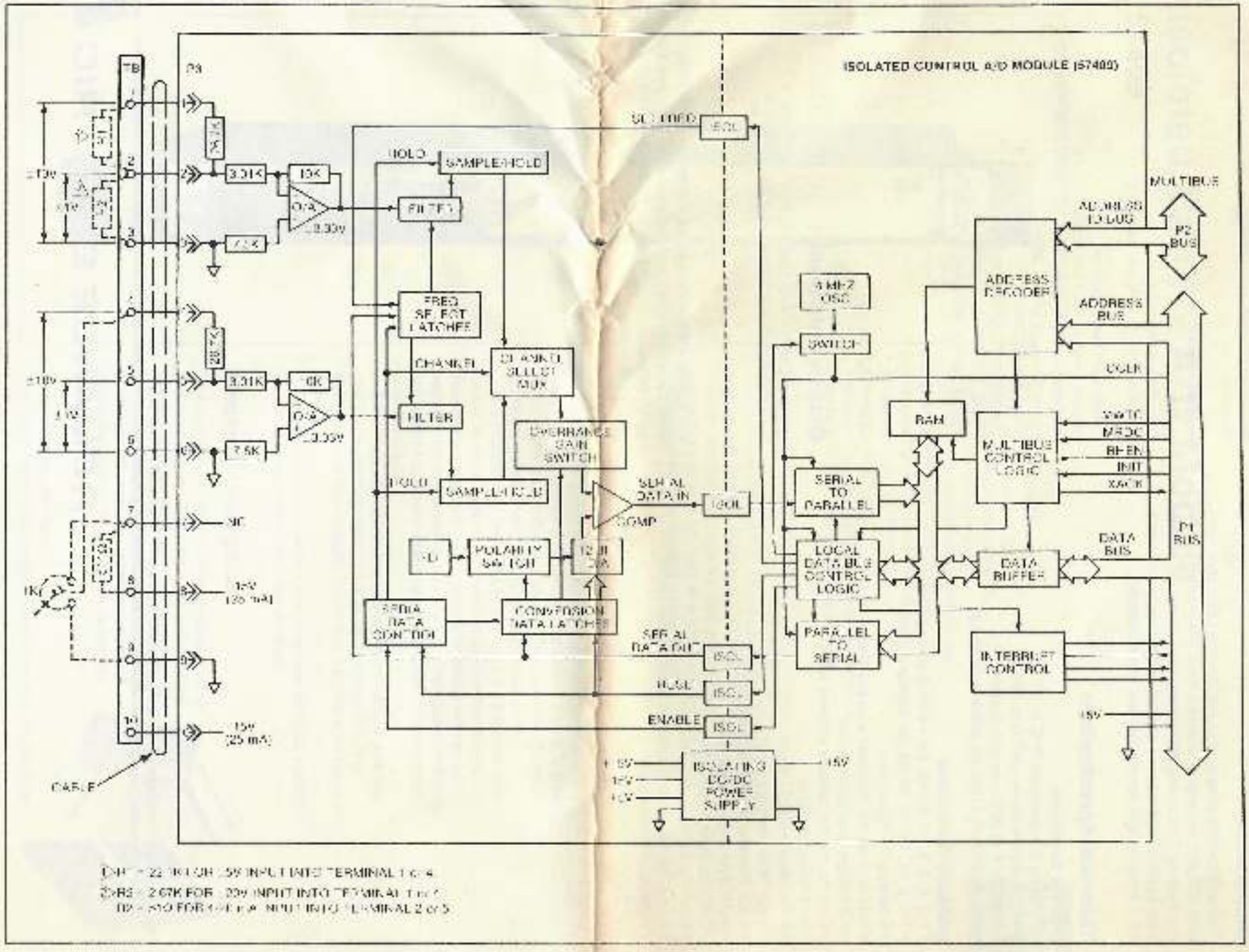

Figure 1 — Block Diagram of Isolated Control A/D Module

Diagnostics

The only built-in diagnostics are the two LEDs that indicate CCLK is on and/or enabled from this module. To test the module, first check the isolated power supply outputs, then connect appropriate signals to the inputs and use a CRT Programmer to monitor and force registers.

Technical Specifications

Ambient Conditions
Operating temperature: 0° C to 55° C
Storage temperature: -40° C to 85° C
Humidity: 5 to 90% non-condensing
Altitude: 3300 ft. (1000 m) without derating

Backplane Connections
P1-3, 4, 5, 6, 81, 82, 83, 84: +5VD-C at 4.82A max
P1-1, 2, 11, 12, 75, 76, 85, 86: Signal common
P1-59 thru 74: Data lines
P1-43 thru 55, 58: Register address lines
P1-57: High byte address line
P1-28, 30, 32, 34: Module address lines
P1-14: Initialize input
P1-19: Read memory input
P1-20: Write memory input
P1-23: Transfer acknowledge output
P1-27: Byte high enable input
P1-31: Constant clock (CCLK)
P1-39, 40, 41, 42: Interrupt lines
P2-5, 9, 10, 14: Module address identification lines
P2-35: Board reset input
P2-59: System watchdog timer OK input

Maximum Module Dissipation
25 watts

Isolated Power Supply
Output: +15V and -15V at 25 mA each
Accuracy: ±1% at 0 to 25 mA
Thermal drift: ± .01% per degree C

Conversion Performance
(Values given in % of full scale, ±½ bit)
Nominal Absolute Accuracy: ±10.000V ±2% = ±4095
Repeatability: 1 LSB = .25%
Linearity: ± .025%
Thermal drift: .015% per degree C
Offset: = 79mV to = 55mV max
Update period: 500 μsec to 32.7675 sec

Dimensions
Height: 11½"
Width: 1½"
Depth: 7⅝"

Ordering Information

Isolated Control A/D Module: Part No. 57109
Terminal Board and Cable: Part No. 61217-R

For further information about the Reliance Electric Distributed Control System, contact your local Reliance Electric Sales Office or call toll free 1-800-245-4501. (In Ohio call 1-800-245-4497.)

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